


LCFC Confidential

Customer Product name
E14 Gen 6 Intel/E16 Gen 2 Intel

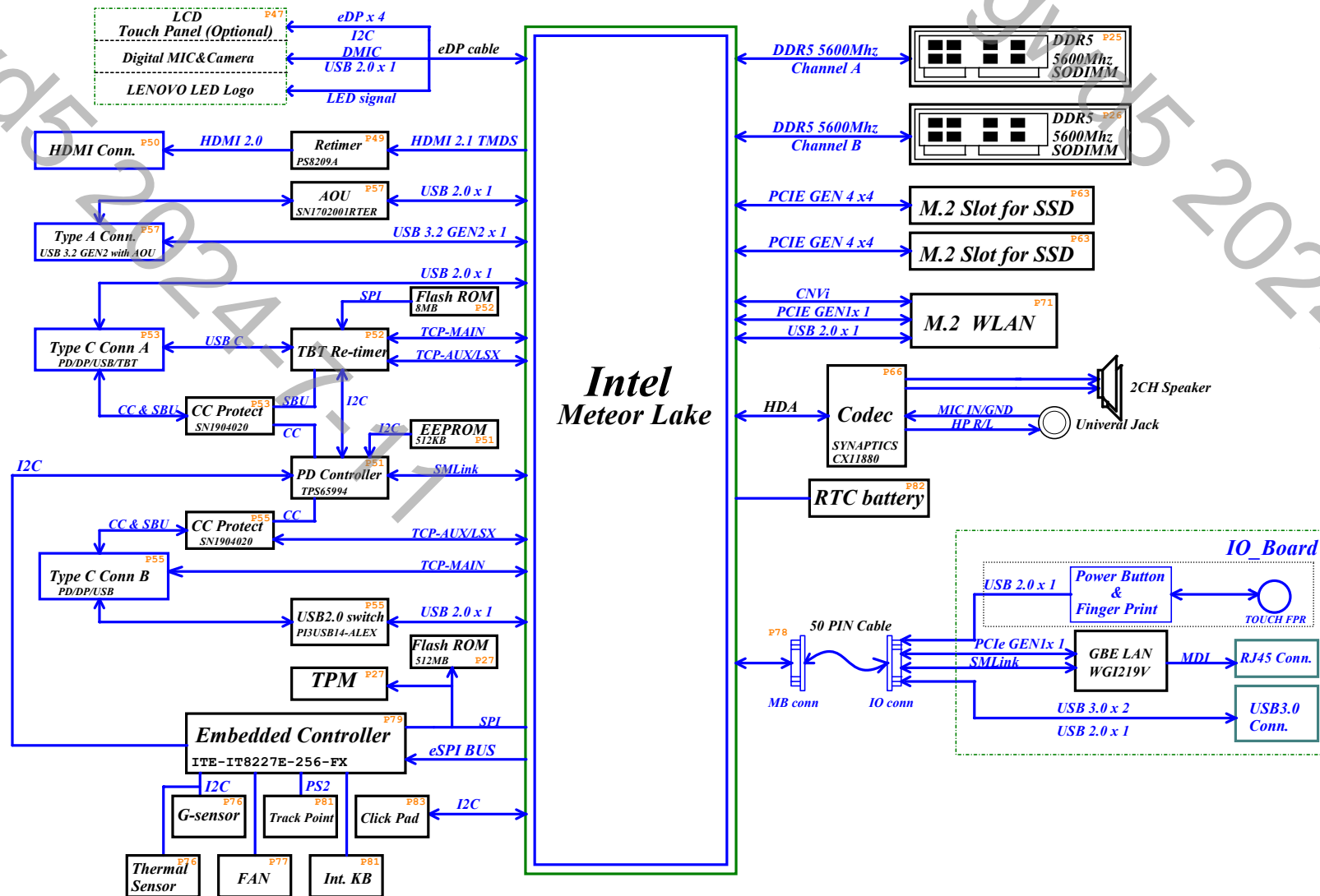
Project Code:
LE460/LE620

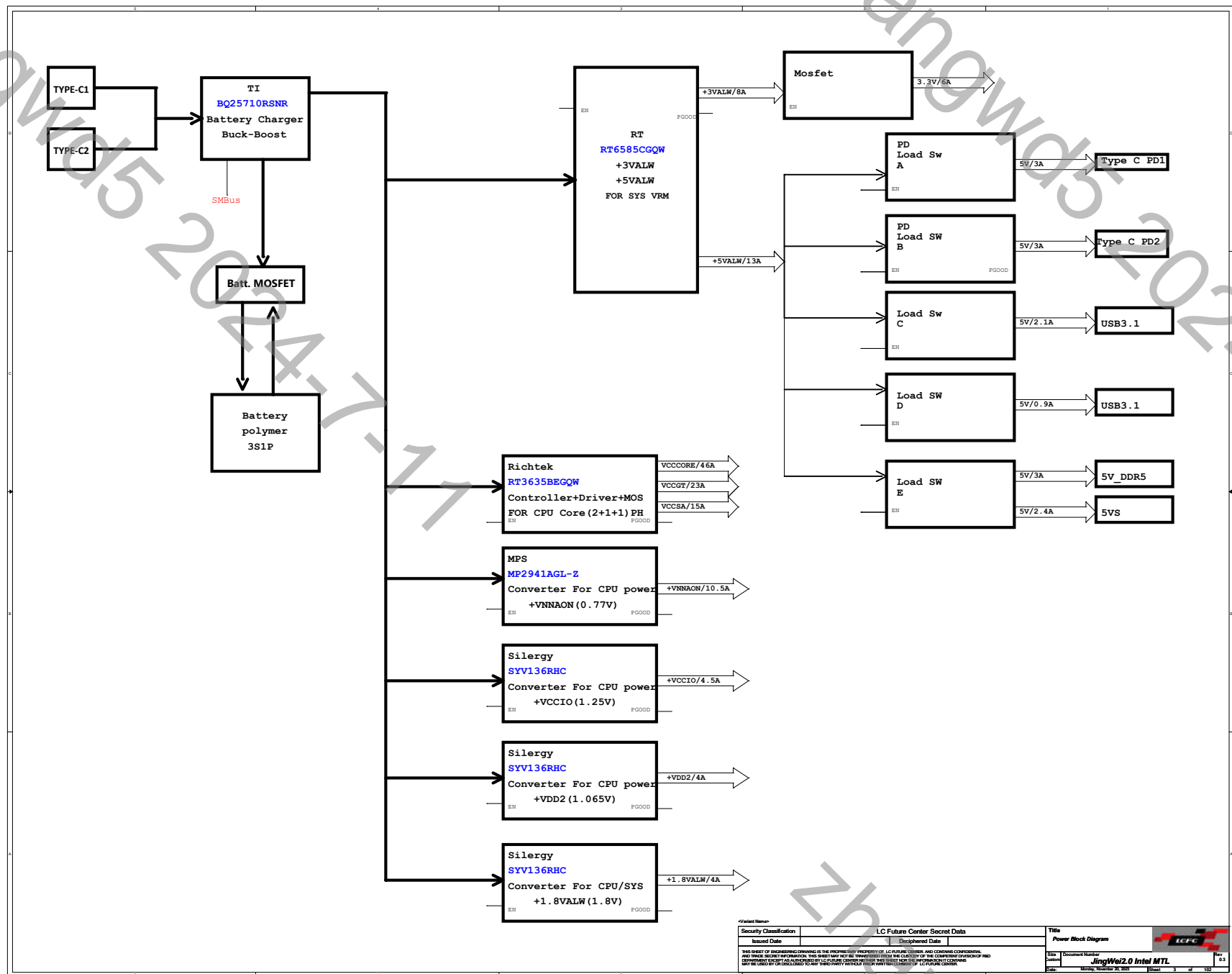
Board Number:
NM-F861

Customer Project name:
Jing Wei 2.0 Intel MTL

Security Classification	LC Future Center Secret Data		Title	
Issued Date	2023/10/26	Deciphered Date	2023/10/31	COVER PAGE
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Custom	JingWei2.0 Intel MTL	0.3		
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Intel Meteor Lake





Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane State	V13B+ +3VL +5VL	+5VALW +3VALW	+3VALW_PCH +1.8VALW	1.2V +VCCST_CPU	+5VS +3VS +1.8VS
S0	O	O	O	O	O
S0Ix	O	O	O	O	O
S4/S5 DC	O	O	O	X	X
S4/S5 DEEP SLEEP	O	O	X	X	X
S4/S5 AC	O	O	O	X	X
S4/S5 AC ONLY	O	O	O	X	X

SMBUS Control Table

EC SMBus address

Device	Address
SMBus0 G-Sensor(LIS2DWLTR)	0011_000
PMIC	0x35
SMBus1 Battery	0001_011
Charger	0001_001
PD	TBD
SMBus4 HDMI Retimer	0x10-0x2F
Thermal Sensor(NCT7718)	1001_100
Audio Codec	NC
SMBus5 Expand	TBD
Thermal Sensor(F75303M)	1001_101

PCH SMBus & I2C address

Device	Address
SMB SO-DIMM	1010_000
SML0 BB Re-timer	0X56
LAN	0XC8
SML1 PD	0X23/27
I2C0 Click Pad	TBD
I2C1 Touch Panel	TBD

HSIO Matrix

HSIO PORT	Function
USB2.0	1 Type-C Port
	2 AOU USB
	3 IOB USB
	4 NC
	5 NC
	6 Finger Printer
	7 Camera
	8 NC
	9 TBT4 TYPE-C
	10 WLAN_BT
USB3.0	1 USB3.2 IOB
	2 NC
	3 NC
	4 NC
PCH PCIE3	5 LAN
	6 NC
	7 NC
	8 WLAN
	9
	10 SSD1
	11
	12
CPU PCIE4	17 SSD2
	18
	19
	20
CPU PCIE4	13
	14 NC
	15
	16
CPU PCIE5	21-24 NC
	25-28
CPU DDI	A eDP Port
	B HDMI Port
CPU TCP	0 Type-C Port
	1 USB3.2 AOU
	2 TBT4 TYPE-C
	3 NC

Virtual Symbol_EE

PCB

CPU

PCB_E14@
ZZZ
PCB LE480 NM-F861 REV0 M/B
DA80001EW10

PCB_E16@
ZZZ
PCB LE620 NM-F861 REV0 M/B
DA80001EW10

U15 I7 vpro@
UC1
S IC QG80723058D5 Q47B C0 1.7GHZ BGA QS
SA0000EX810

U15 I7 Non-vpro@
UC1
S IC QG80723058D7 Q47U C0 1.7GHZ BGA QS
SA0000EX710

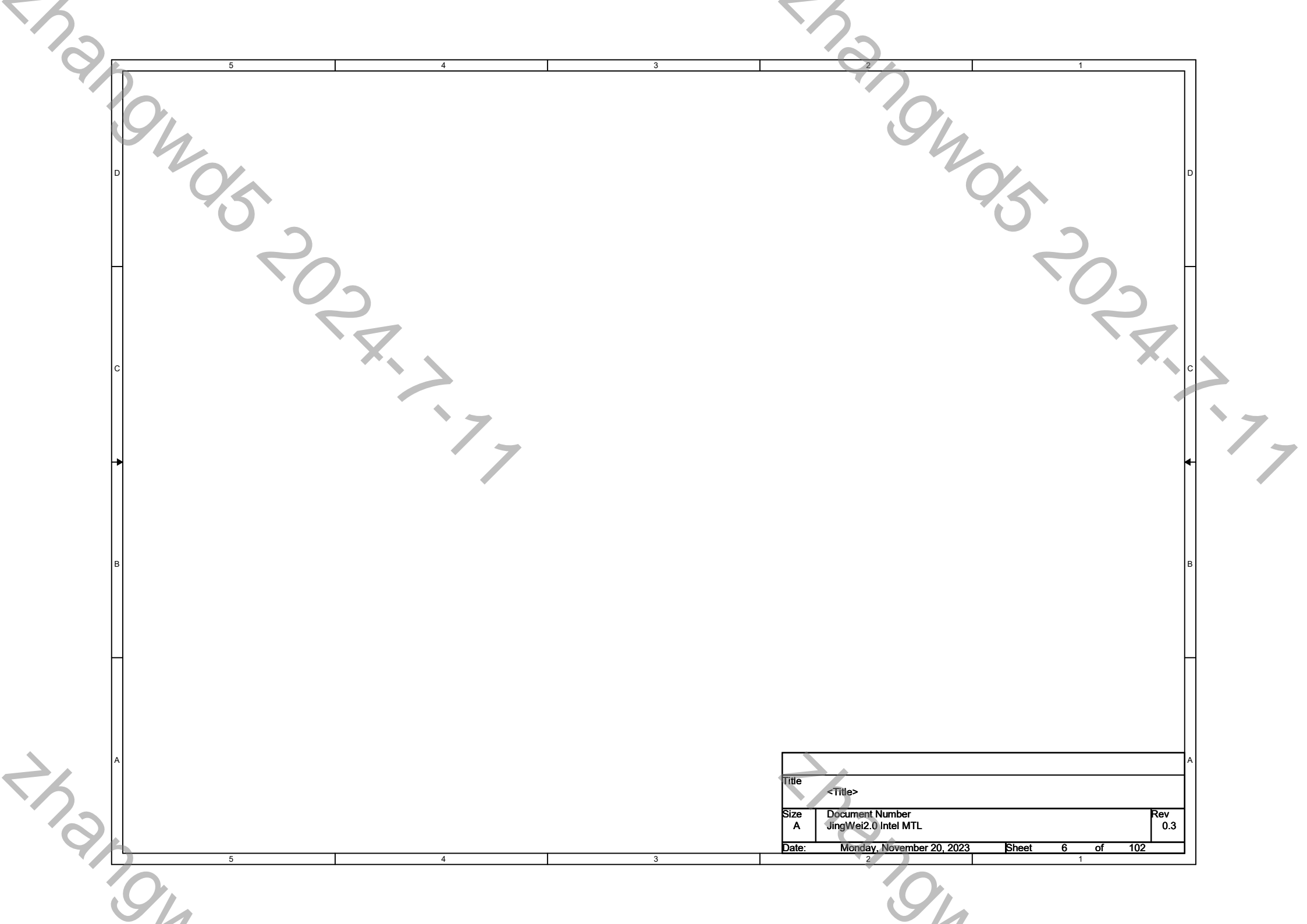
U15 i5 vpro@
UC1
S IC QG80723058D9 Q47T C0 1.6GHZ BGA QS
SA0000EX810

U15 i5 Non-vpro@
UC1
S IC QG80723058D8 Q47W C0 1.3GHZ BGA QS
SA0000EX910

H28 I7 non-vPro@
UC1
S IC QG807230556A Q3TD C0 1.1GHZ BGA QS
SA0000EMT20

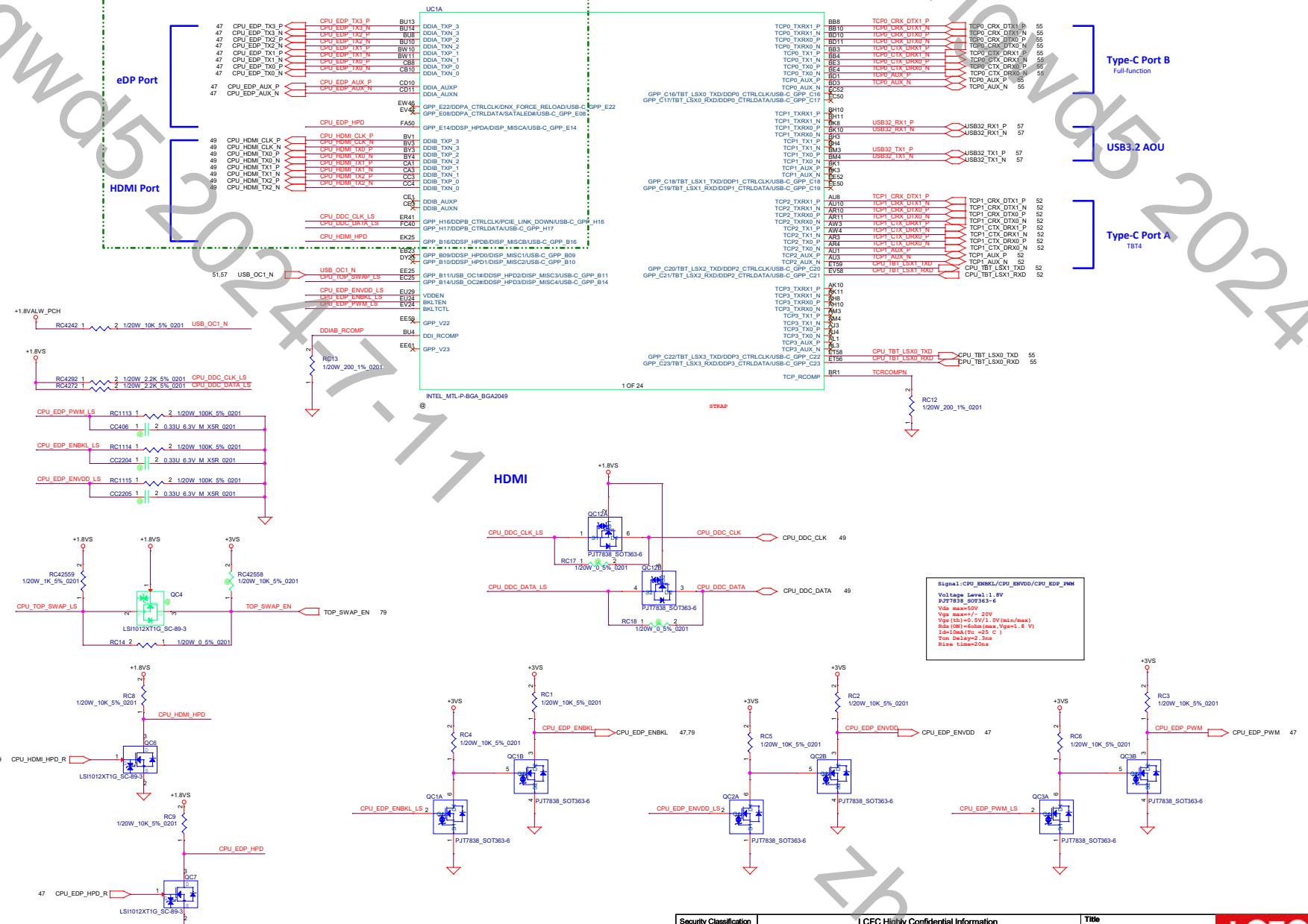
H28 i5 non-vPro@
UC1
S IC QG807230556E Q3TK C0 1.2GHZ BGA QS
SA0000EMV30

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Size	Document Number	Rev	
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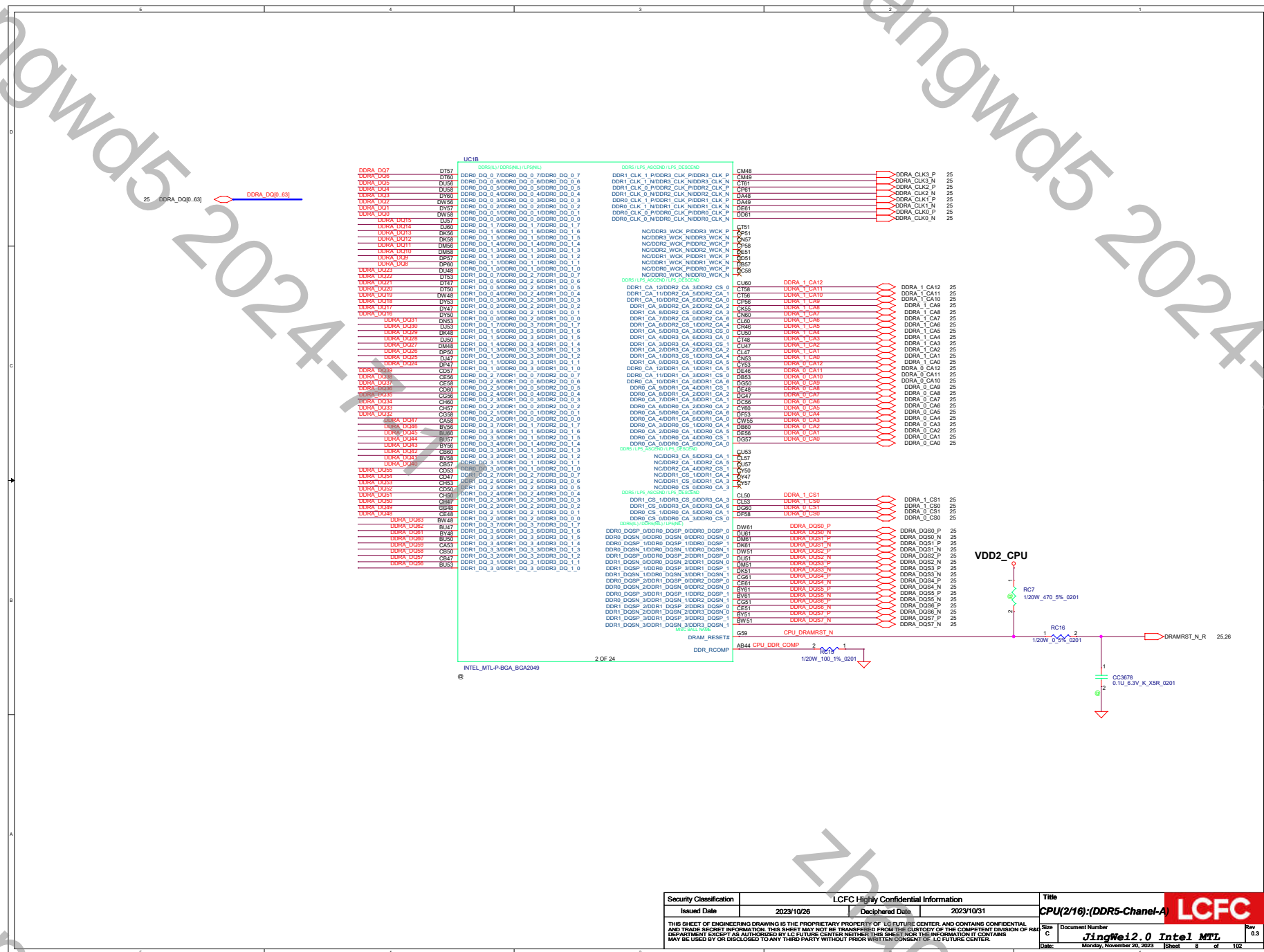


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Size	Document Number	Rev
A	JingWei2.0 Intel MTL	0.3
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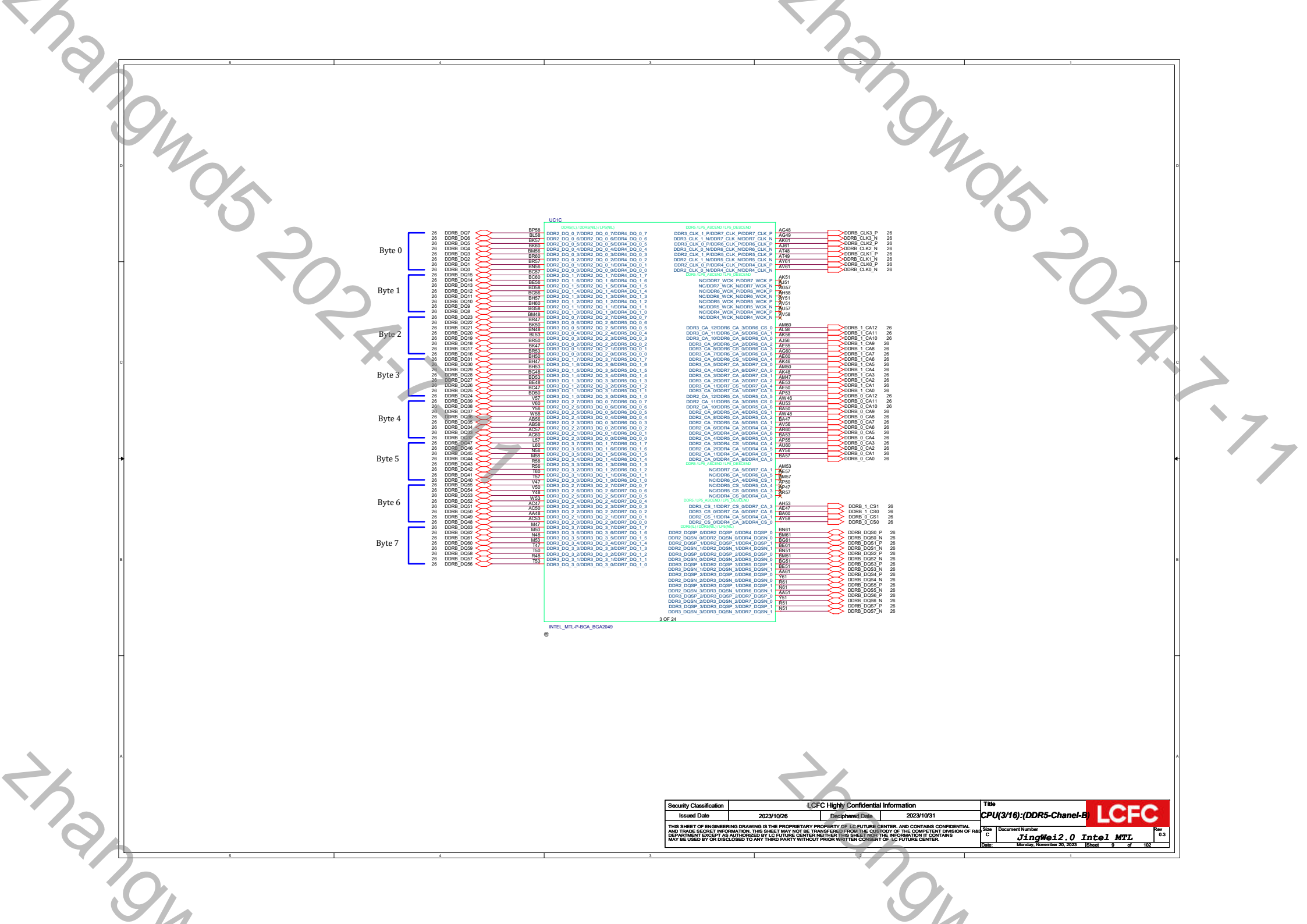
SIT Phase, 交换eDP Port和HDMI Port



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Issued Date	2023/10/26	Deciphered Date	2023/10/31	CPU(1/16):(DDV/EDP/TBT)	
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				JingWei2.0 Intel MTL	8.3
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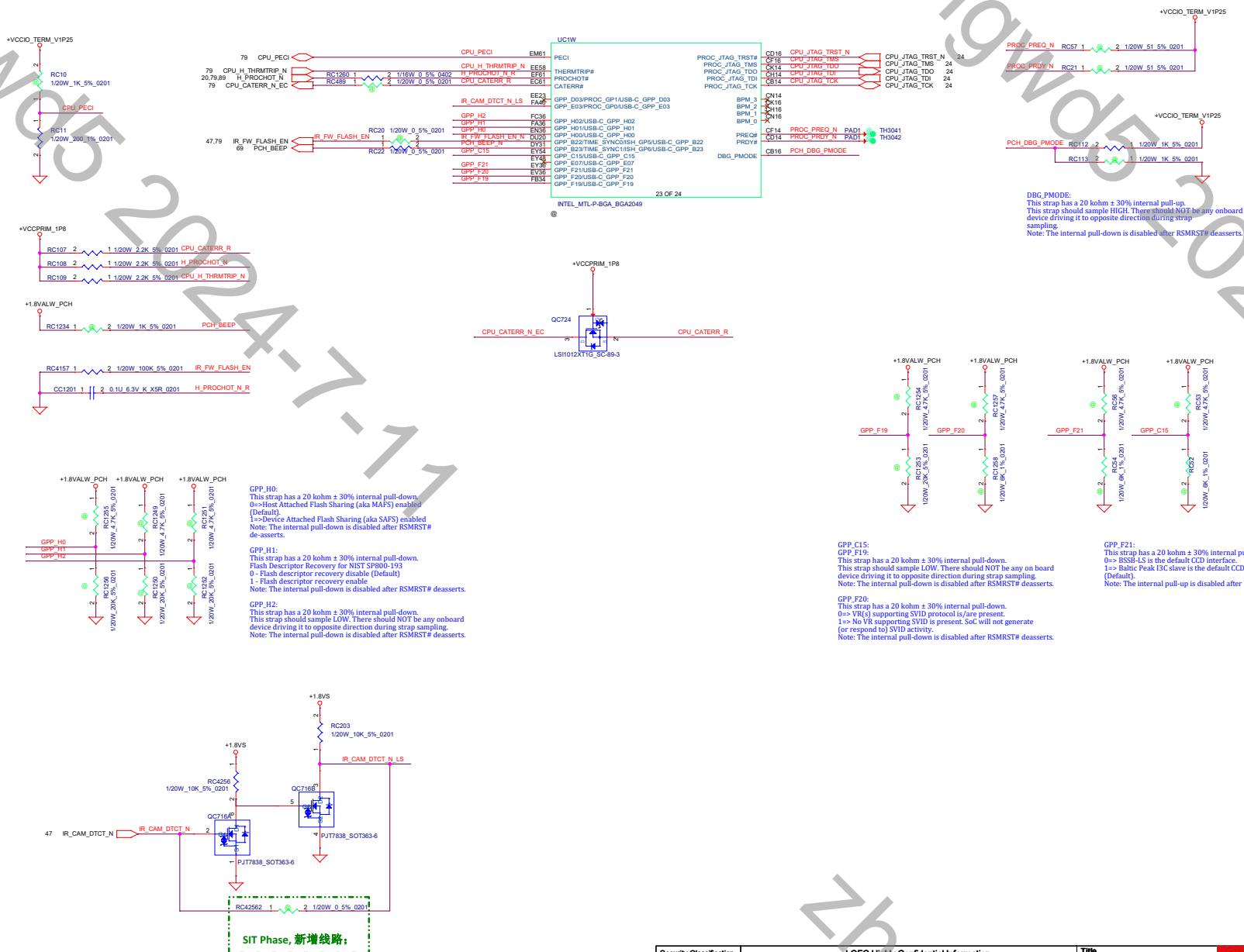
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		UCIC			
		DDR5(LPS_ASCEND)/LPS_N		DDR5(LPS_ASCEND)/LPS_DESCEND	
Byte 0	26	DDR5_DQ0	DDR5_DQ0_0_7DDR5_DQ0_0_7	DDR5_DQ0	DDR5_DQ0_0_7DDR5_DQ0_0_7
	26	DDR5_DQ1	DDR5_DQ1_0_7DDR5_DQ1_0_7	DDR5_DQ1	DDR5_DQ1_0_7DDR5_DQ1_0_7
	26	DDR5_DQ2	DDR5_DQ2_0_7DDR5_DQ2_0_7	DDR5_DQ2	DDR5_DQ2_0_7DDR5_DQ2_0_7
	26	DDR5_DQ3	DDR5_DQ3_0_7DDR5_DQ3_0_7	DDR5_DQ3	DDR5_DQ3_0_7DDR5_DQ3_0_7
Byte 1	26	DDR5_DQ4	DDR5_DQ4_0_7DDR5_DQ4_0_7	DDR5_DQ4	DDR5_DQ4_0_7DDR5_DQ4_0_7
	26	DDR5_DQ5	DDR5_DQ5_0_7DDR5_DQ5_0_7	DDR5_DQ5	DDR5_DQ5_0_7DDR5_DQ5_0_7
	26	DDR5_DQ6	DDR5_DQ6_0_7DDR5_DQ6_0_7	DDR5_DQ6	DDR5_DQ6_0_7DDR5_DQ6_0_7
	26	DDR5_DQ7	DDR5_DQ7_0_7DDR5_DQ7_0_7	DDR5_DQ7	DDR5_DQ7_0_7DDR5_DQ7_0_7
Byte 2	26	DDR5_DQ8	DDR5_DQ8_0_7DDR5_DQ8_0_7	DDR5_DQ8	DDR5_DQ8_0_7DDR5_DQ8_0_7
	26	DDR5_DQ9	DDR5_DQ9_0_7DDR5_DQ9_0_7	DDR5_DQ9	DDR5_DQ9_0_7DDR5_DQ9_0_7
	26	DDR5_DQ10	DDR5_DQ10_0_7DDR5_DQ10_0_7	DDR5_DQ10	DDR5_DQ10_0_7DDR5_DQ10_0_7
	26	DDR5_DQ11	DDR5_DQ11_0_7DDR5_DQ11_0_7	DDR5_DQ11	DDR5_DQ11_0_7DDR5_DQ11_0_7
Byte 3	26	DDR5_DQ12	DDR5_DQ12_0_7DDR5_DQ12_0_7	DDR5_DQ12	DDR5_DQ12_0_7DDR5_DQ12_0_7
	26	DDR5_DQ13	DDR5_DQ13_0_7DDR5_DQ13_0_7	DDR5_DQ13	DDR5_DQ13_0_7DDR5_DQ13_0_7
	26	DDR5_DQ14	DDR5_DQ14_0_7DDR5_DQ14_0_7	DDR5_DQ14	DDR5_DQ14_0_7DDR5_DQ14_0_7
	26	DDR5_DQ15	DDR5_DQ15_0_7DDR5_DQ15_0_7	DDR5_DQ15	DDR5_DQ15_0_7DDR5_DQ15_0_7
Byte 4	26	DDR5_DQ16	DDR5_DQ16_0_7DDR5_DQ16_0_7	DDR5_DQ16	DDR5_DQ16_0_7DDR5_DQ16_0_7
	26	DDR5_DQ17	DDR5_DQ17_0_7DDR5_DQ17_0_7	DDR5_DQ17	DDR5_DQ17_0_7DDR5_DQ17_0_7
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	26	DDR5_DQ27	DDR5_DQ27_0_7DDR5_DQ27_0_7	DDR5_DQ27	DDR5_DQ27_0_7DDR5_DQ27_0_7
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	26	DDR5_DQ29	DDR5_DQ29_0_7DDR5_DQ29_0_7	DDR5_DQ29	DDR5_DQ29_0_7DDR5_DQ29_0_7
	26	DDR5_DQ30	DDR5_DQ30_0_7DDR5_DQ30_0_7	DDR5_DQ30	DDR5_DQ30_0_7DDR5_DQ30_0_7
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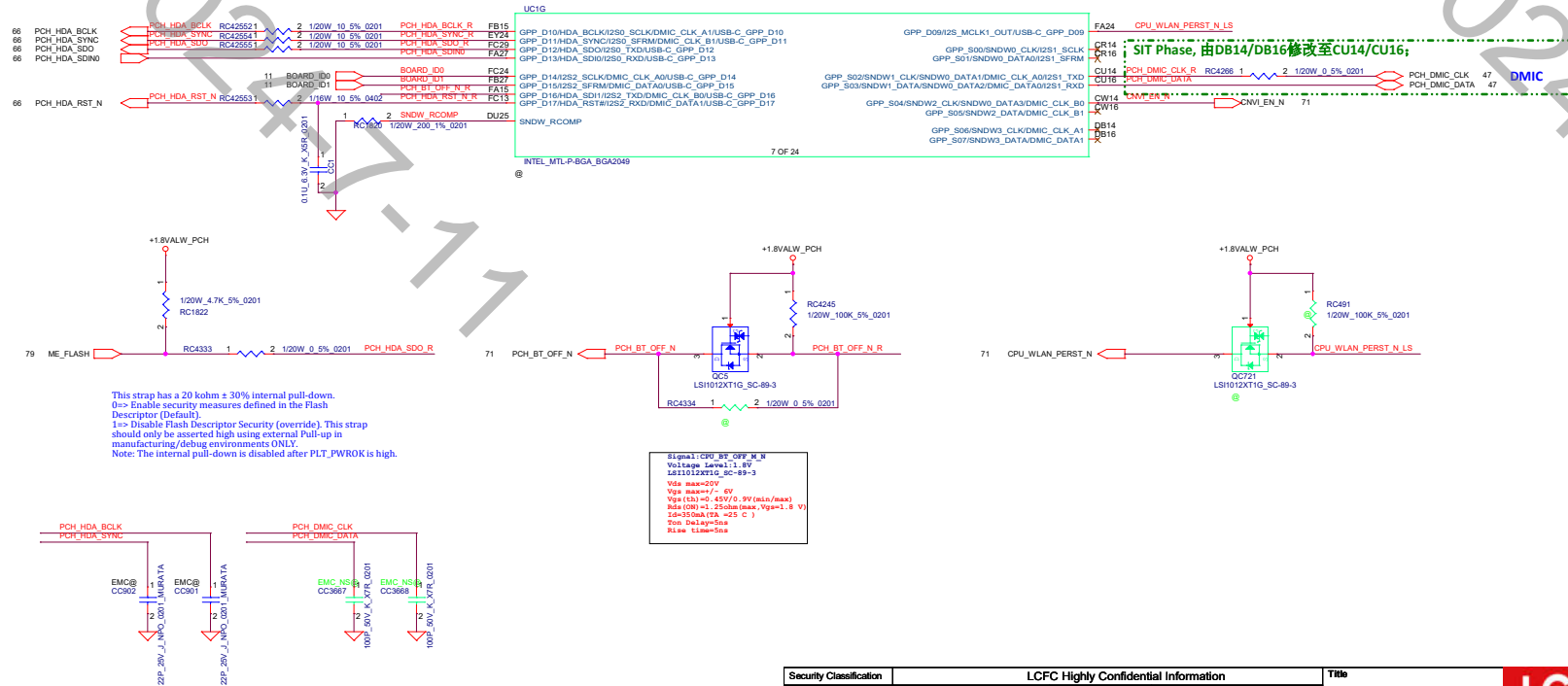
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Security Classification		LCFC Highly Confidential Information		Title	
Issued Date		Deciphered Date		CPU(3/16)-(DDR5-Chanel-B)	
2023/10/26		2023/10/31		LCFC	
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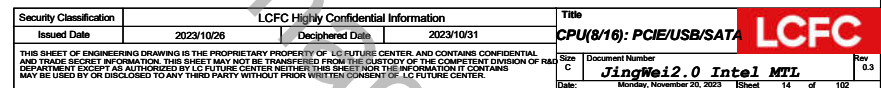



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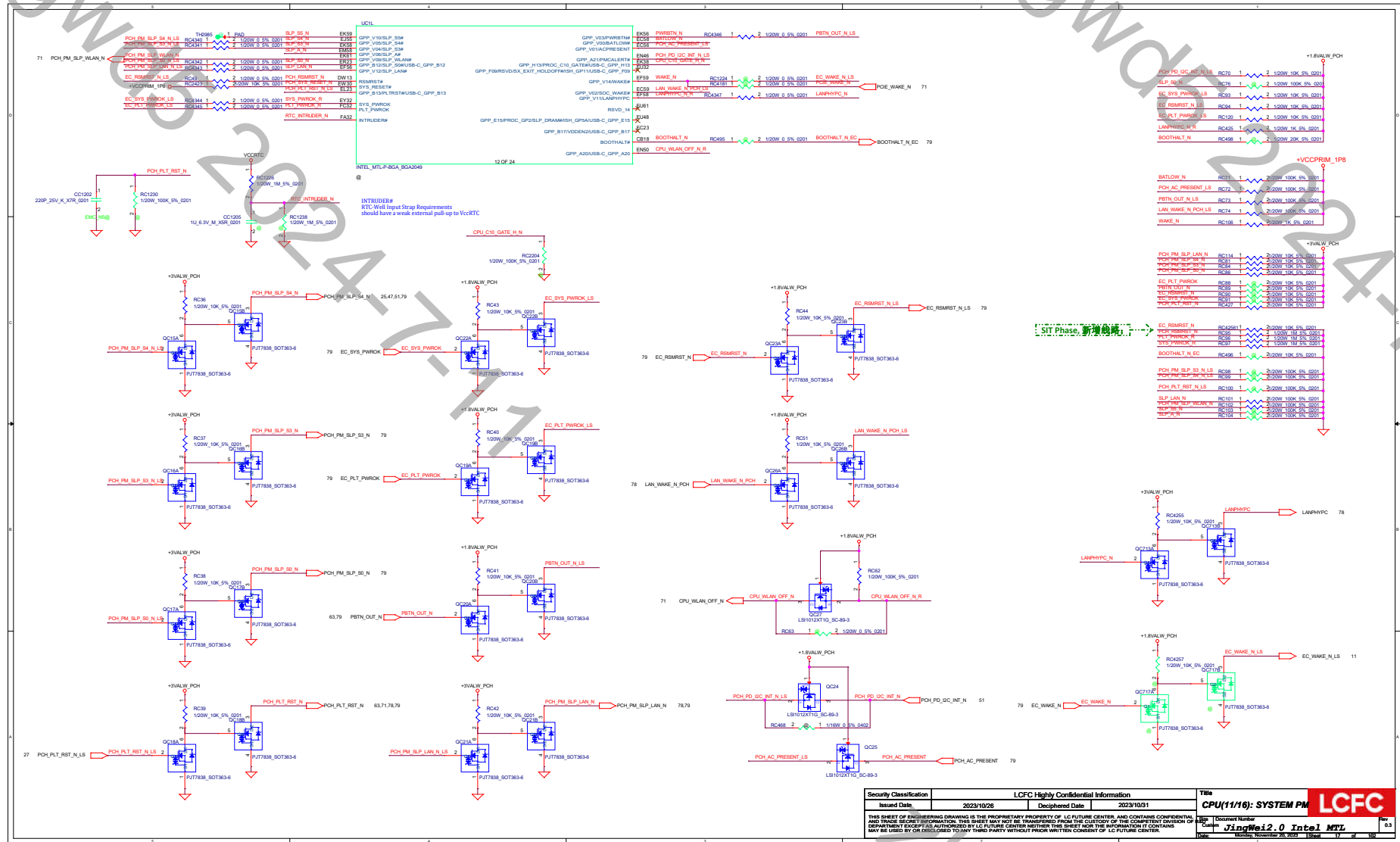
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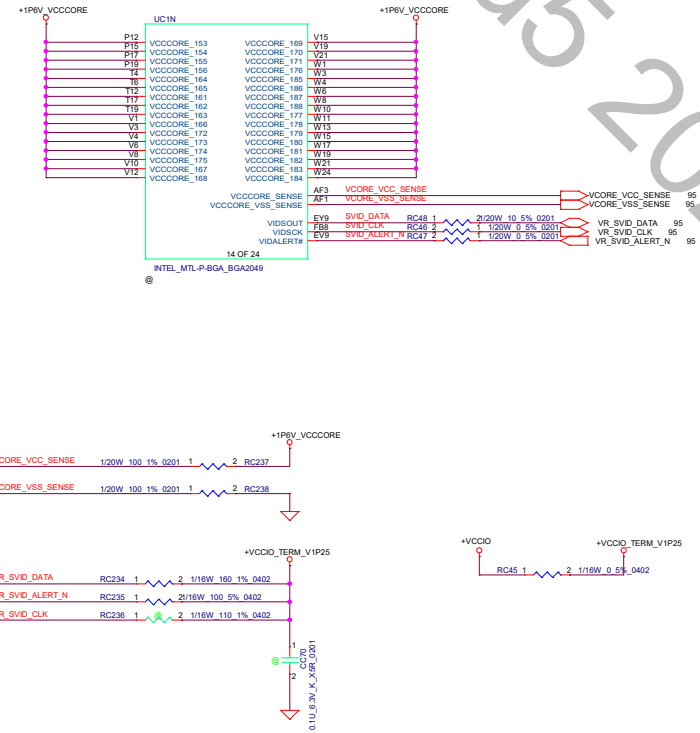
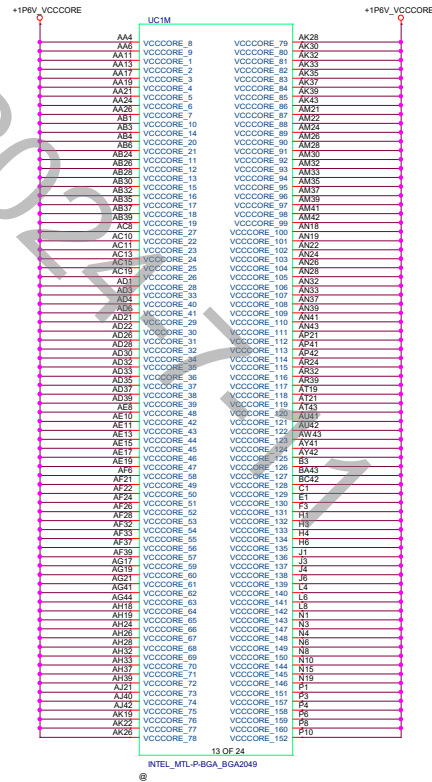


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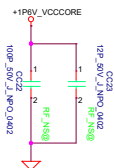


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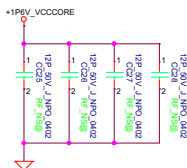




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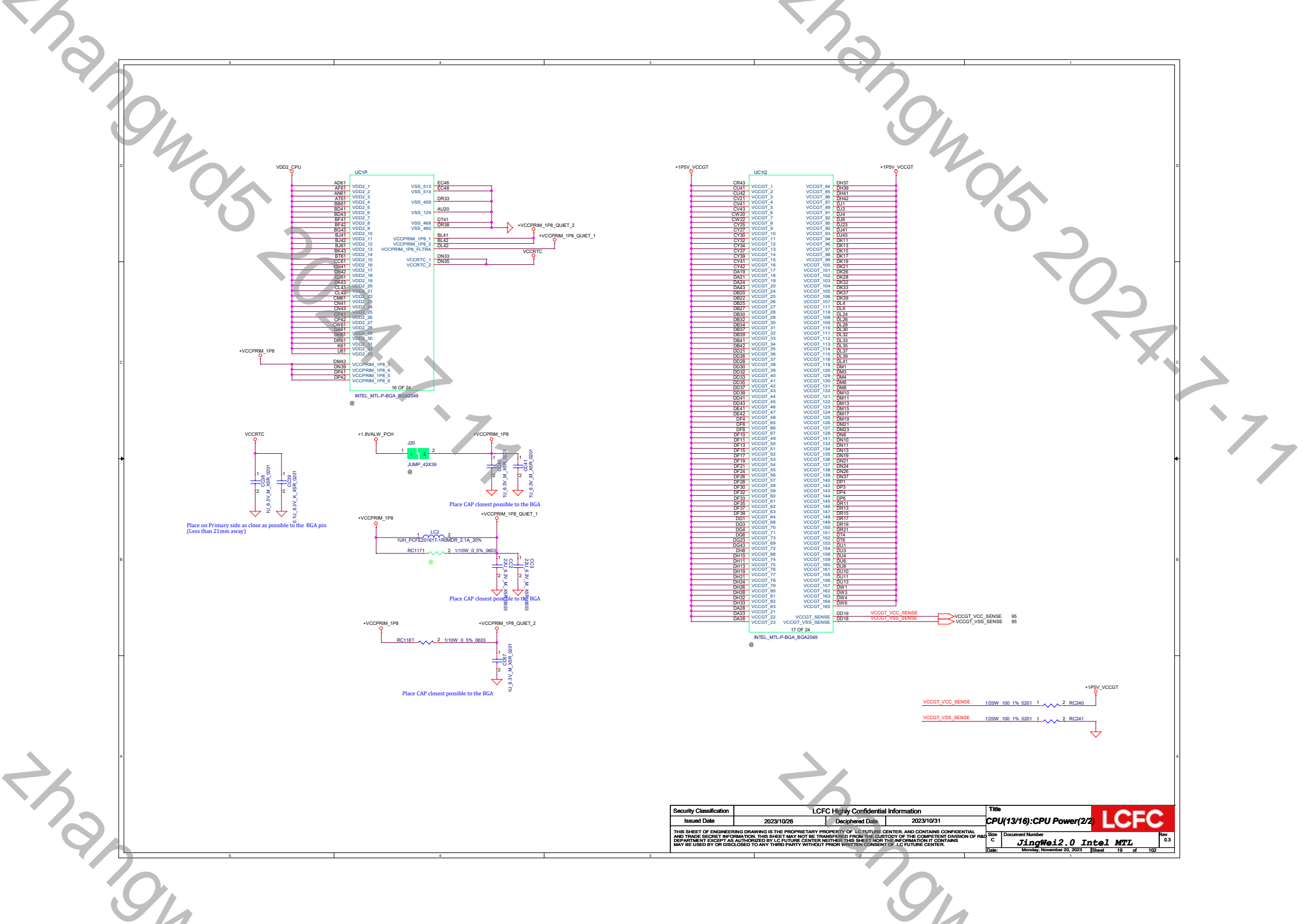


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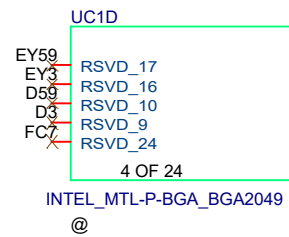


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Issued Date		Deciphered Date		Document Number		JingWei2.0 Intel MTL	
2023/10/26		2023/10/31		Size		New	
C		1		Date		Monday, November 20, 2023	
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Size A		Document Number								Rev 0.3	
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Date:		Monday, November 20, 2023				Sheet		21 of 102			
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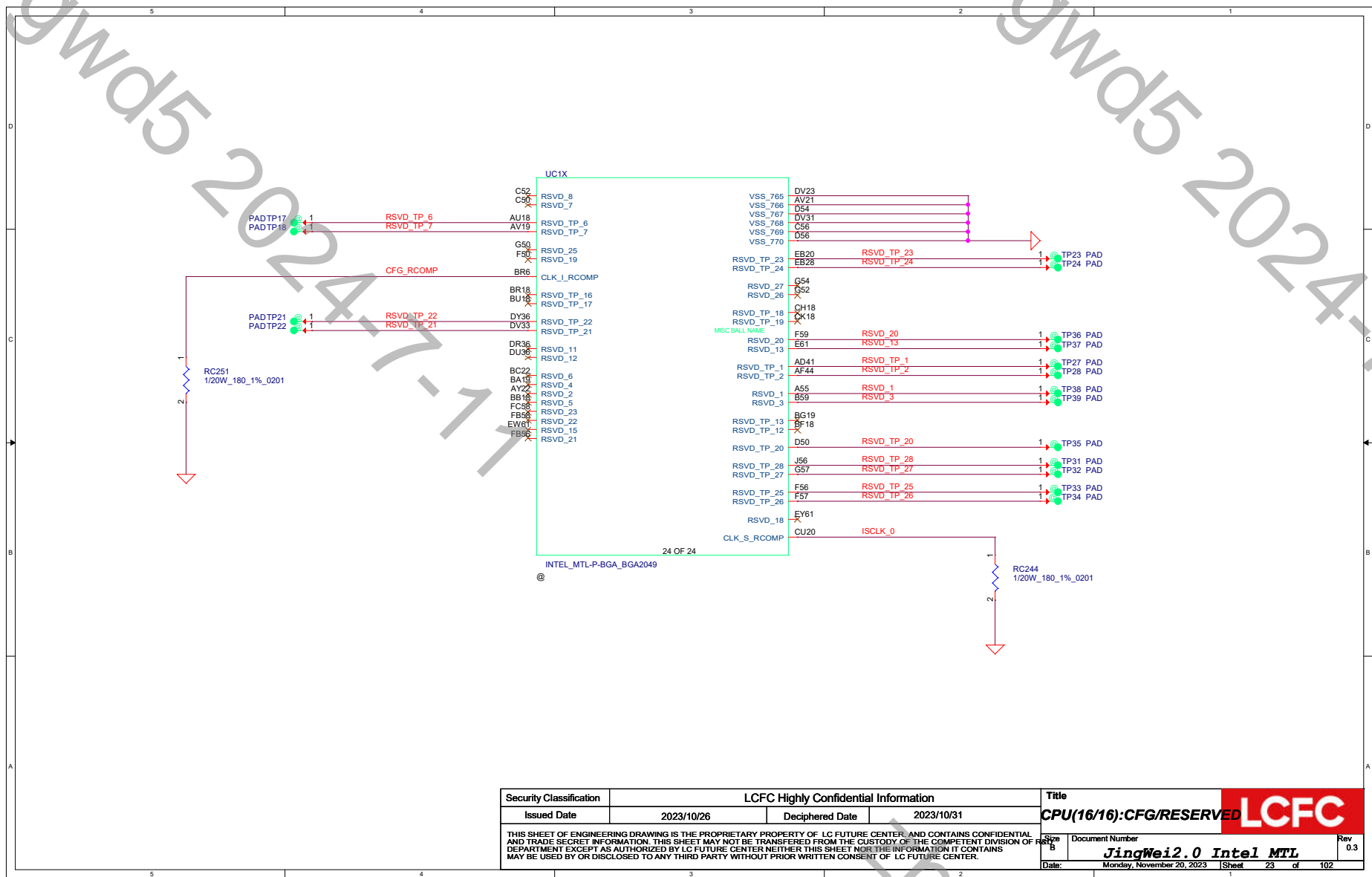


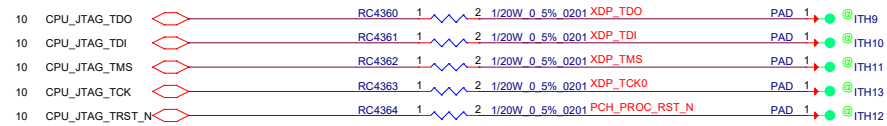
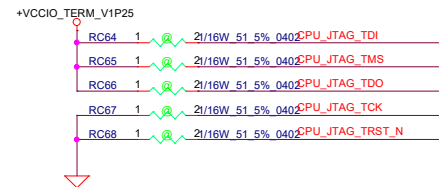
TABLE : CPU ITP DEBUG REPORT


	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

↑
LOGIC

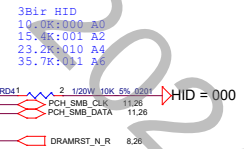
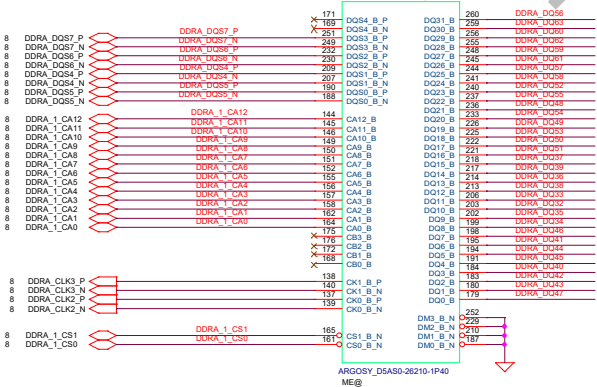
TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

↑
LOGIC

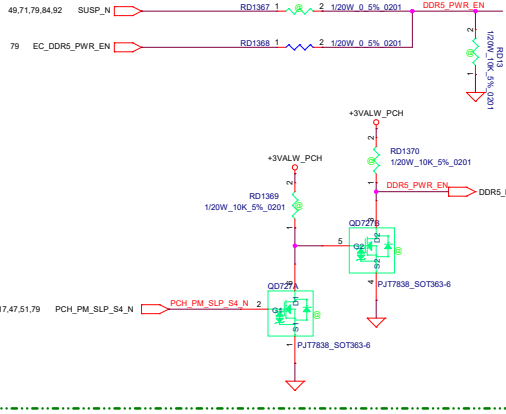
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2023/10/26	Deciphered Date	2023/10/31	CPU Debug		
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				B	JingWei2.0 Intel MTL	0.3
				Date:	Monday, November 20, 2023	Sheet 24 of 102



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8 DDRA_DQ[0..63]
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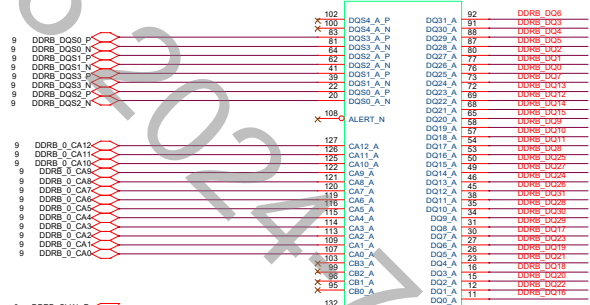
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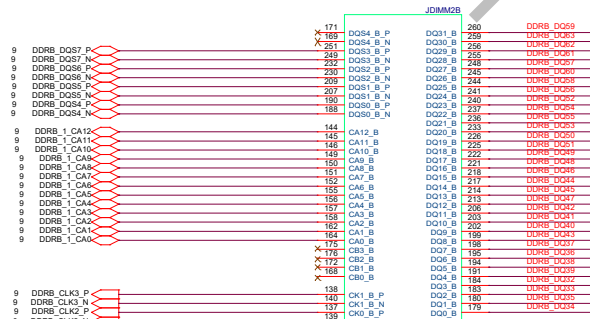
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DDR5 SO-DIMM2

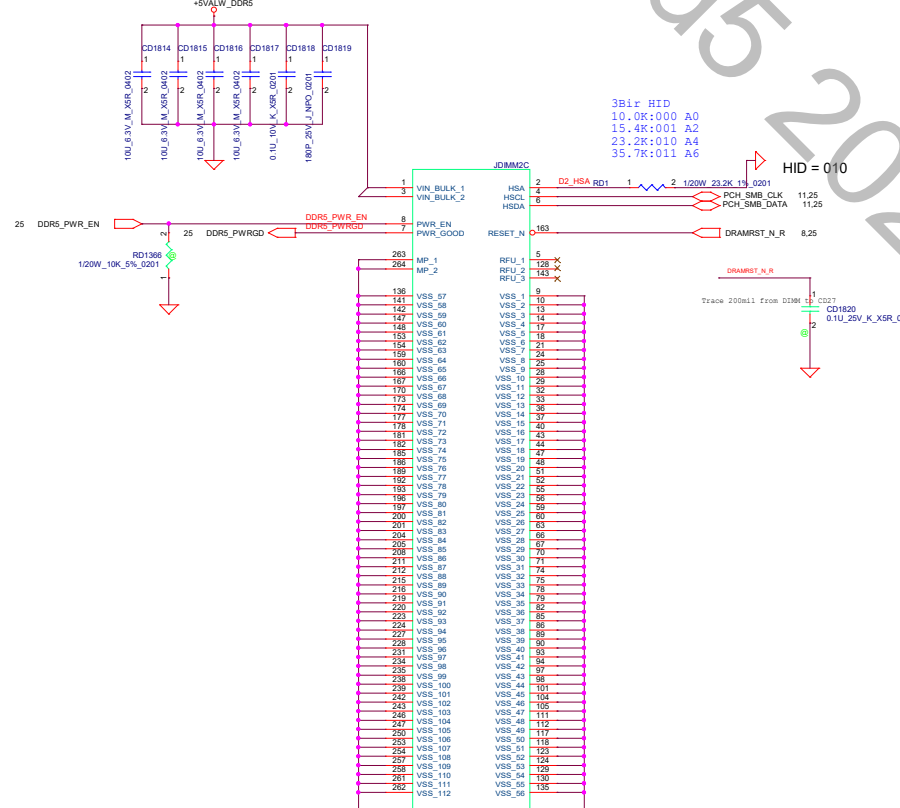
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ME@

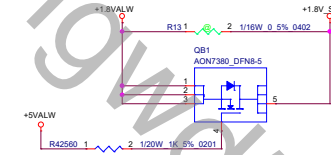
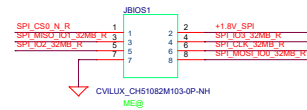


ARGOSY_D5AS0-26210-1P40
ME@



ARGOSY_D5AS0-26210-1P40
ME@

SPI ROM



TPM IC

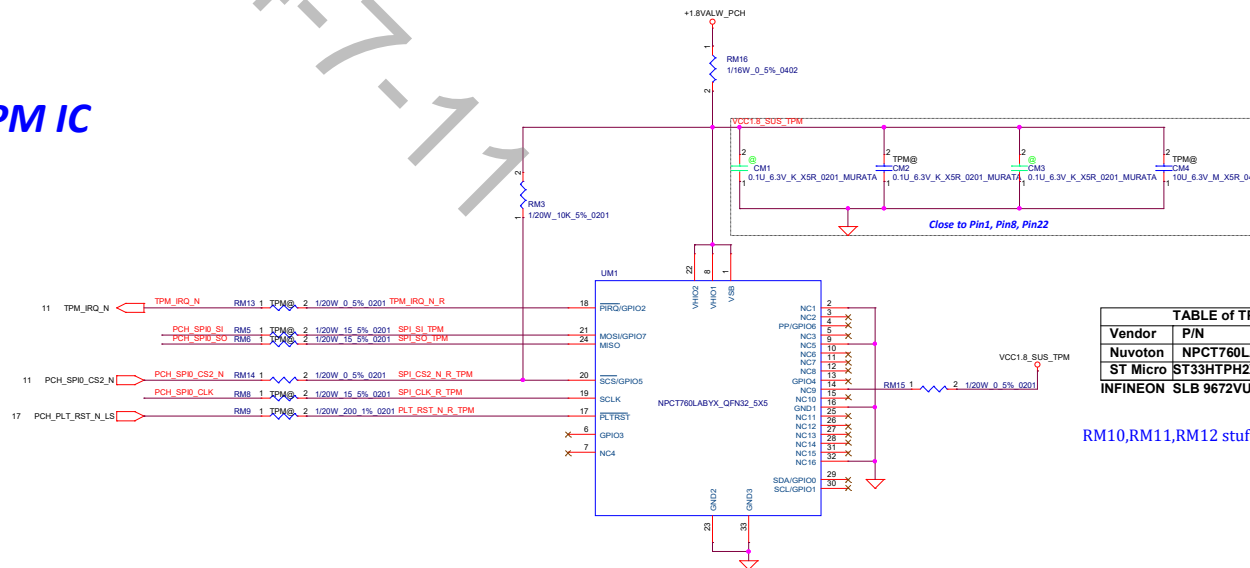



TABLE of TPM (UM1)		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT760LAAYX	SA0000C3000
ST Micro	ST33HTPH2X32AHE0	SA0000C8600
INFINEON	SLB 9672VU2.0 FW15.20SA0000C3300	

RM10,RM11,RM12 stuff when using INFINEON TPM


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Title		SPI ROM/TPM	
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			File	M0000_20230720_18200		15 of 104

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					JingWei2.0	Intel MTL	

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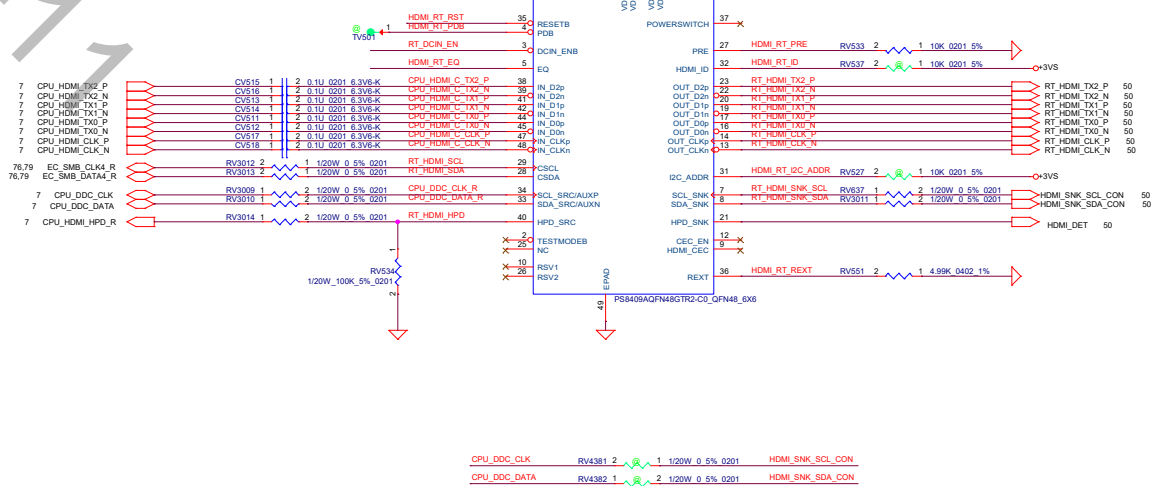
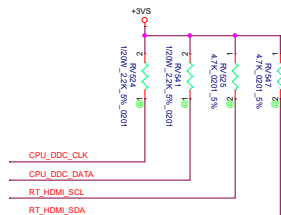
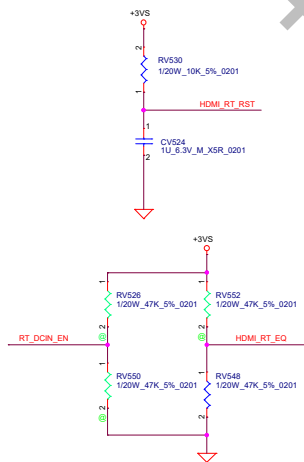
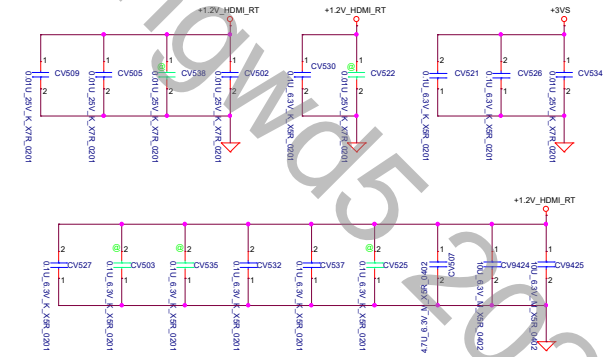
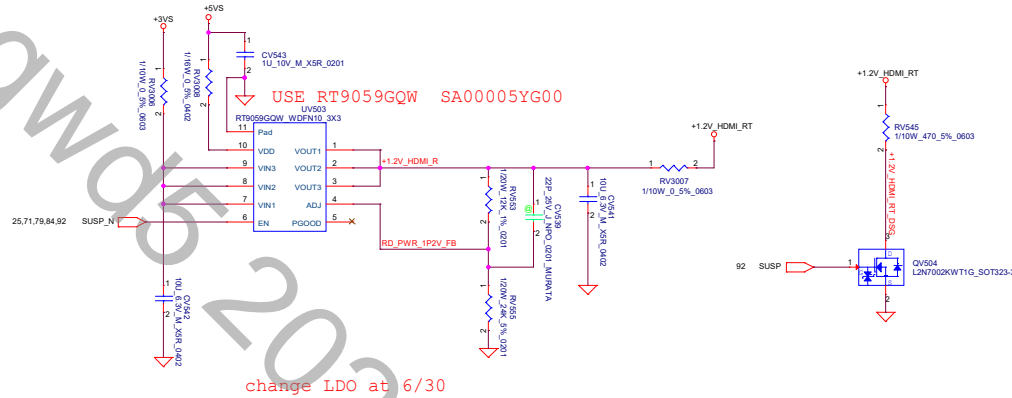
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				Date	Sheet
				Monday, November 20, 2023	46 of 102

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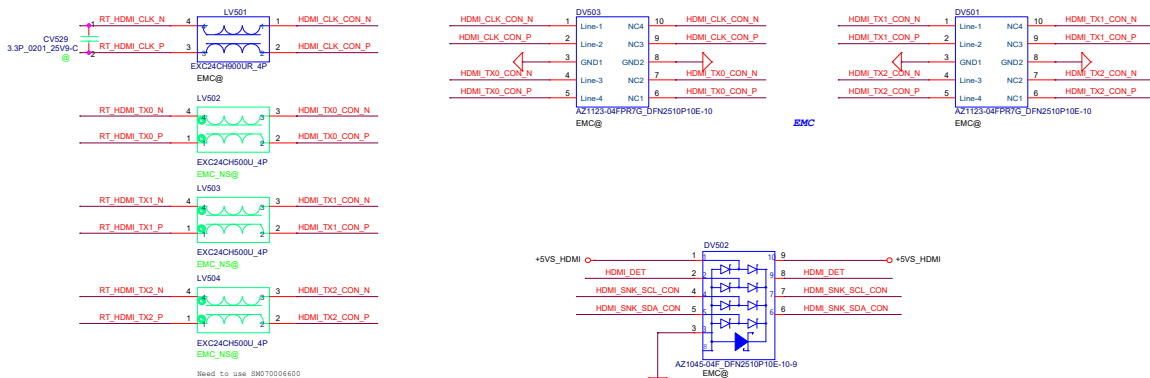
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Issued Date			2023/10/26		Deciphered Date		2023/10/31	
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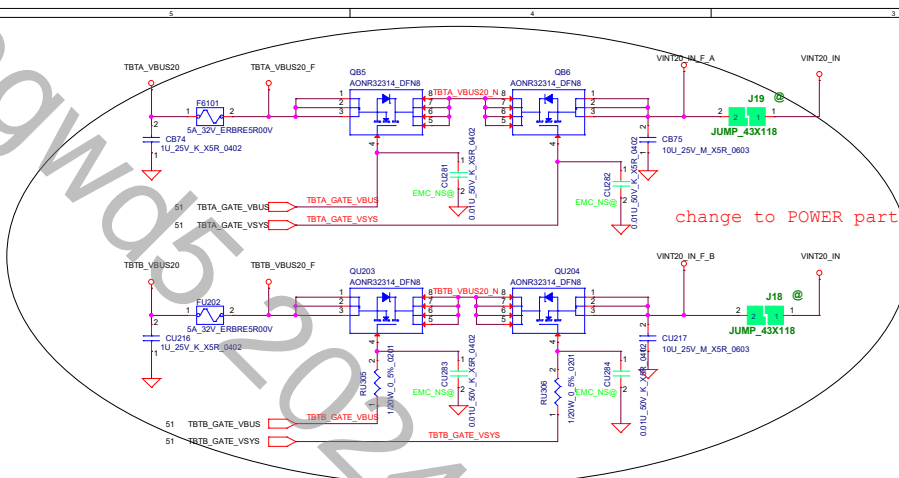
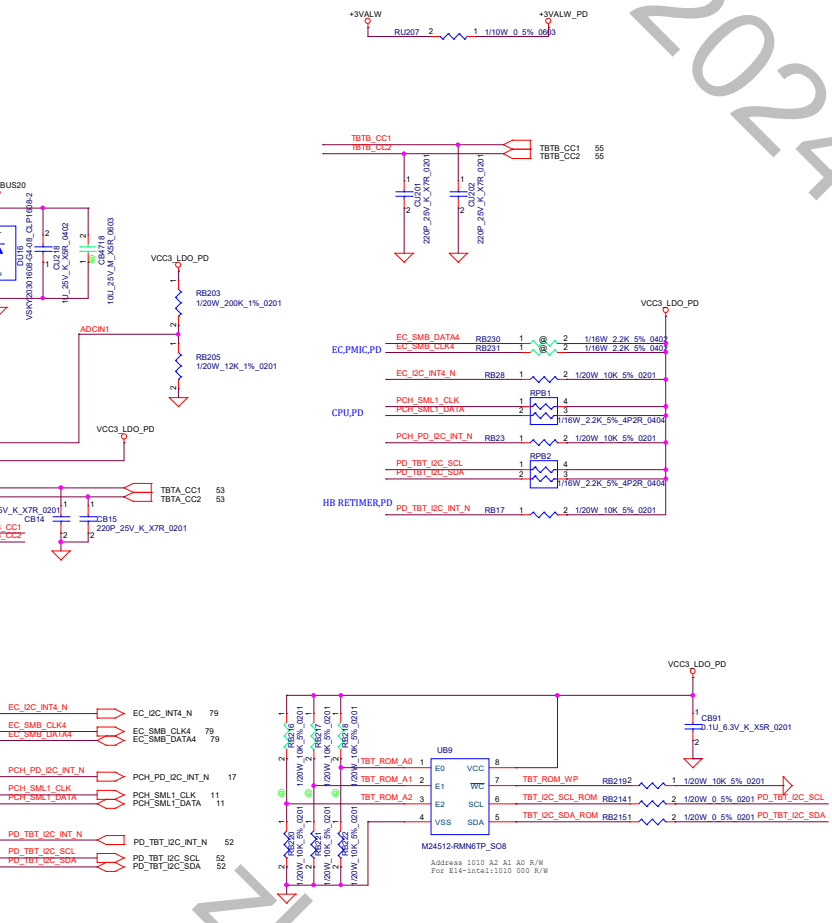
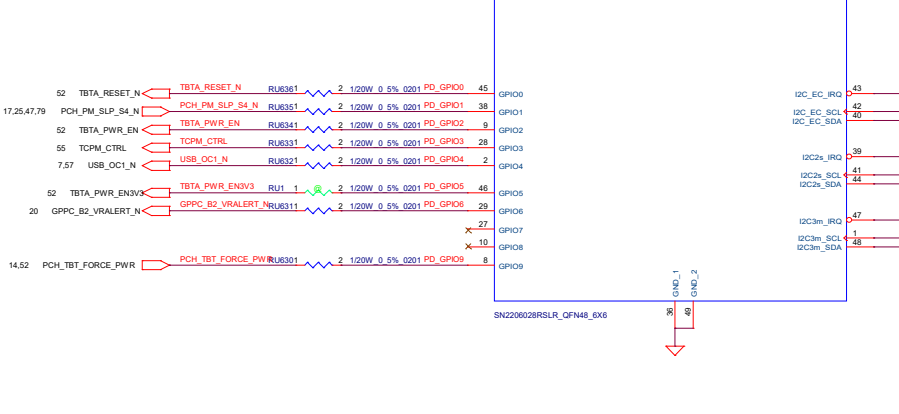
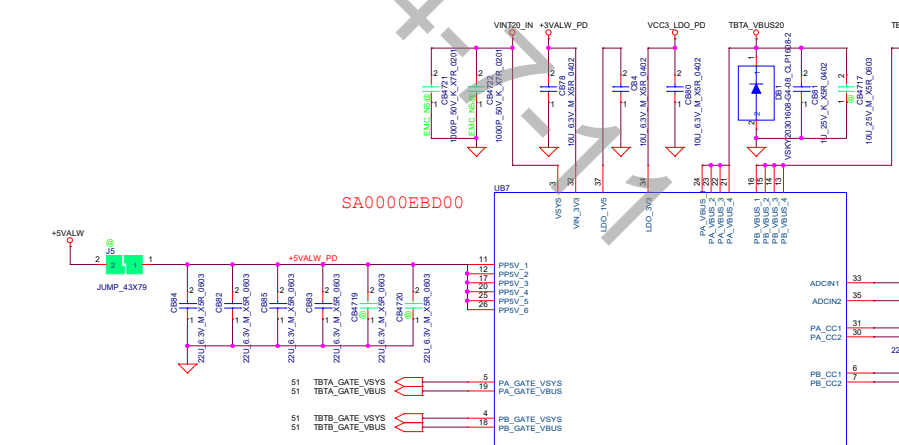


TABLE I2C Addressing

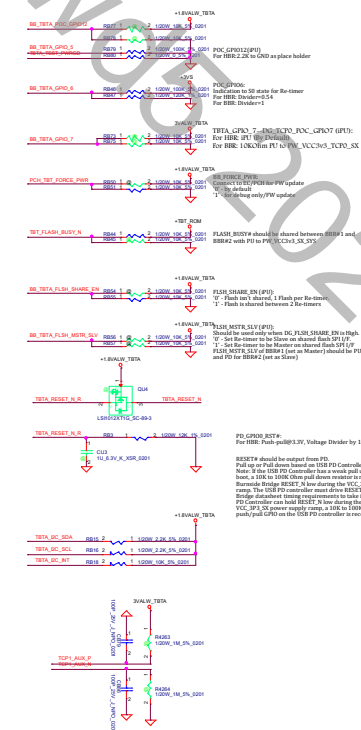
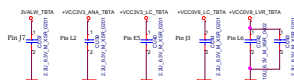
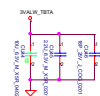
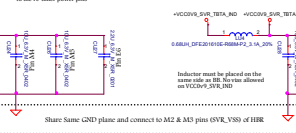
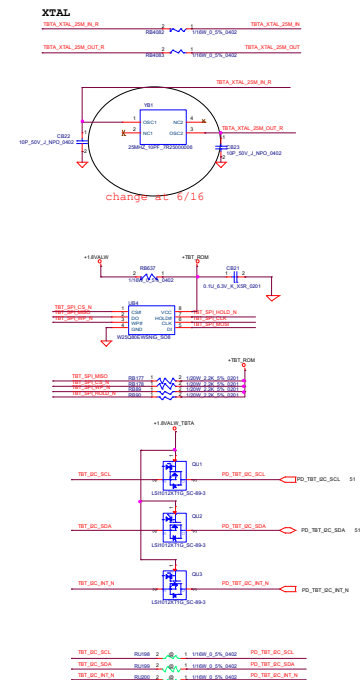
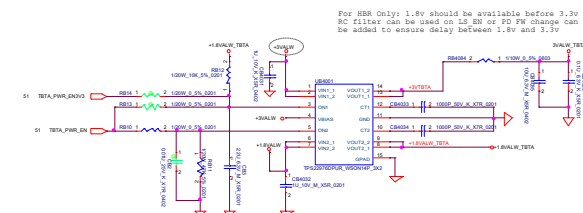
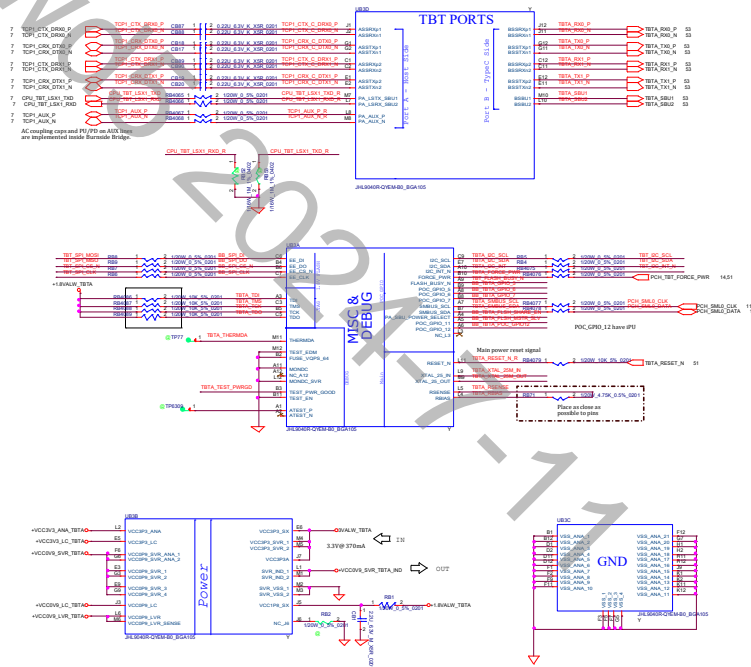
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I2C3	Master: PD	TBTA_PORT F.B.D.
	Slave: RT	TBTA_PORT F.B.D.

Table T: Device Configuration using ADDRESS and ADDRESS

Device Functional Modes (continued)



Security Classification	LC Future Center Secret Data	Title	PD_Controller
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		C	JingWei2.0 Intel MTL
		Date	Monday, November 20, 2023
		Sheet	51 of 102



PD_GPIO_0 = 7;
For HBR: Push-pull@3.3V, Voltage Divider by 10K&12K to 1.8V

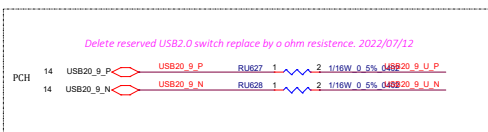
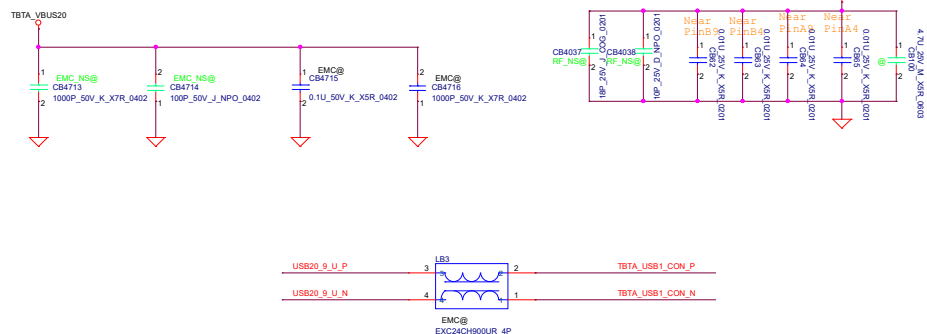
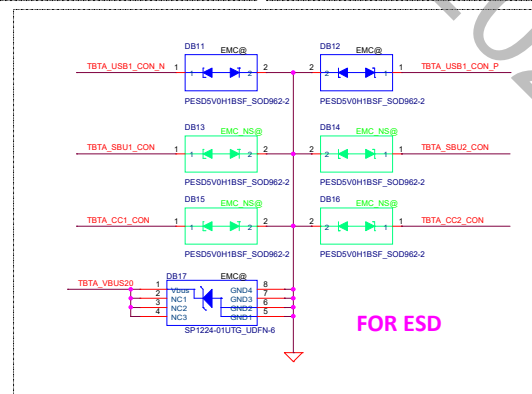
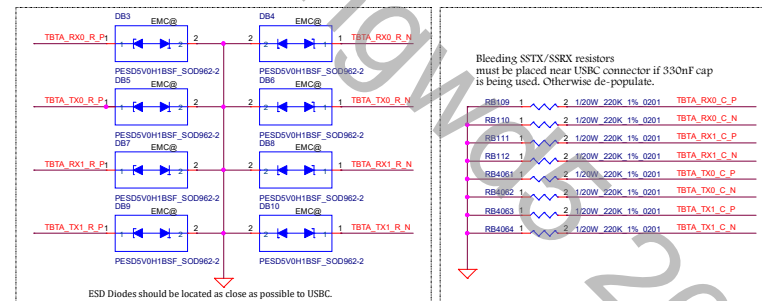
RESET# should be output from PD.
 Pull up or Pull down based on USB PD Controller **GPIO** design.
 Note: If the USB PD Controller has a weak pull up present during its boot, a 10K to 100K Ohm pull down resistor is required to keep the Burnside Bridge **RESET#** Low during the VCC_3P3_SX power supply ramp. The USB PD controller must drive **RESET#** (meeting the Burnside Bridge datasheet timing requirements) to take it out of reset. If the USB PD Controller can hold **RESET#** Low during the Burnside Bridge **VCC_3P3_SX** power supply ramp, a 10K to 100K Ohm pull up and push/pull **GPIO** on the USB PD controller is recommended.

For HBR Only: 1.8v should be available before 3.3v
RC filter can be used on LS EN or PD FW change can
be added to ensure delay between 1.8v and 3.3v

tor must be placed on the side as BE. No vis allowed
V/D: 5/28/2020


Share same GND plane and connect to M2 & M3 pins (SVR_VSS) of HBR

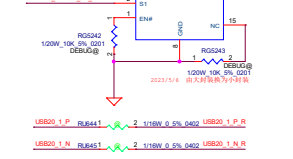
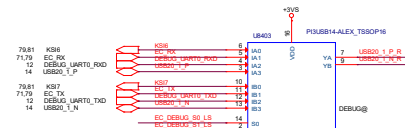
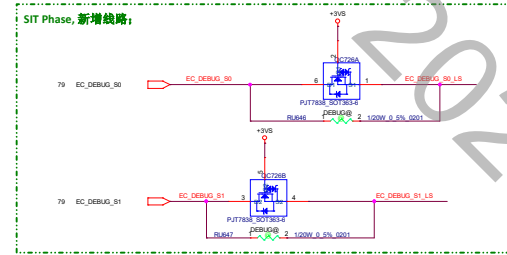
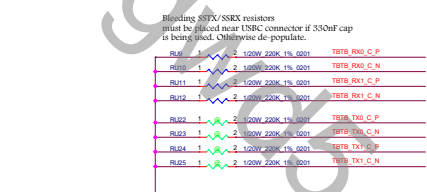
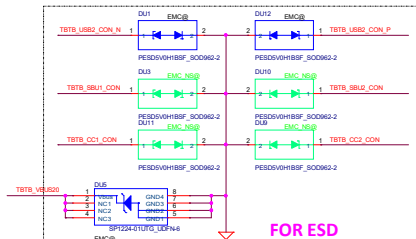
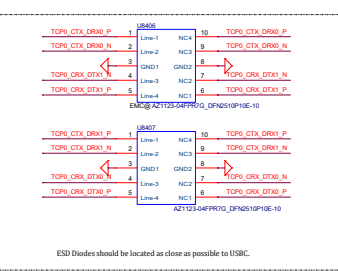
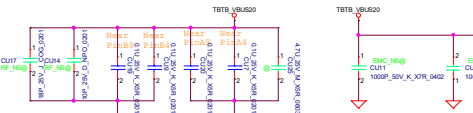
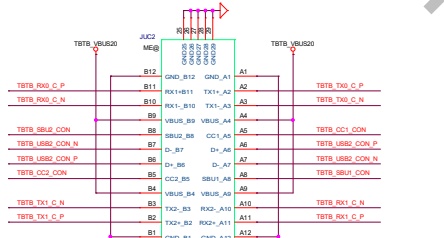
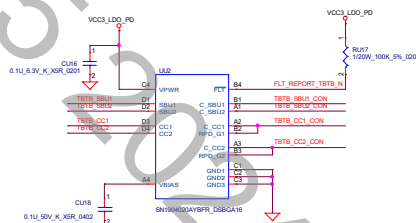
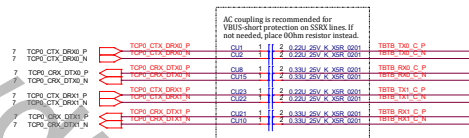
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Doc Version	Doc Date		2023/02/08		



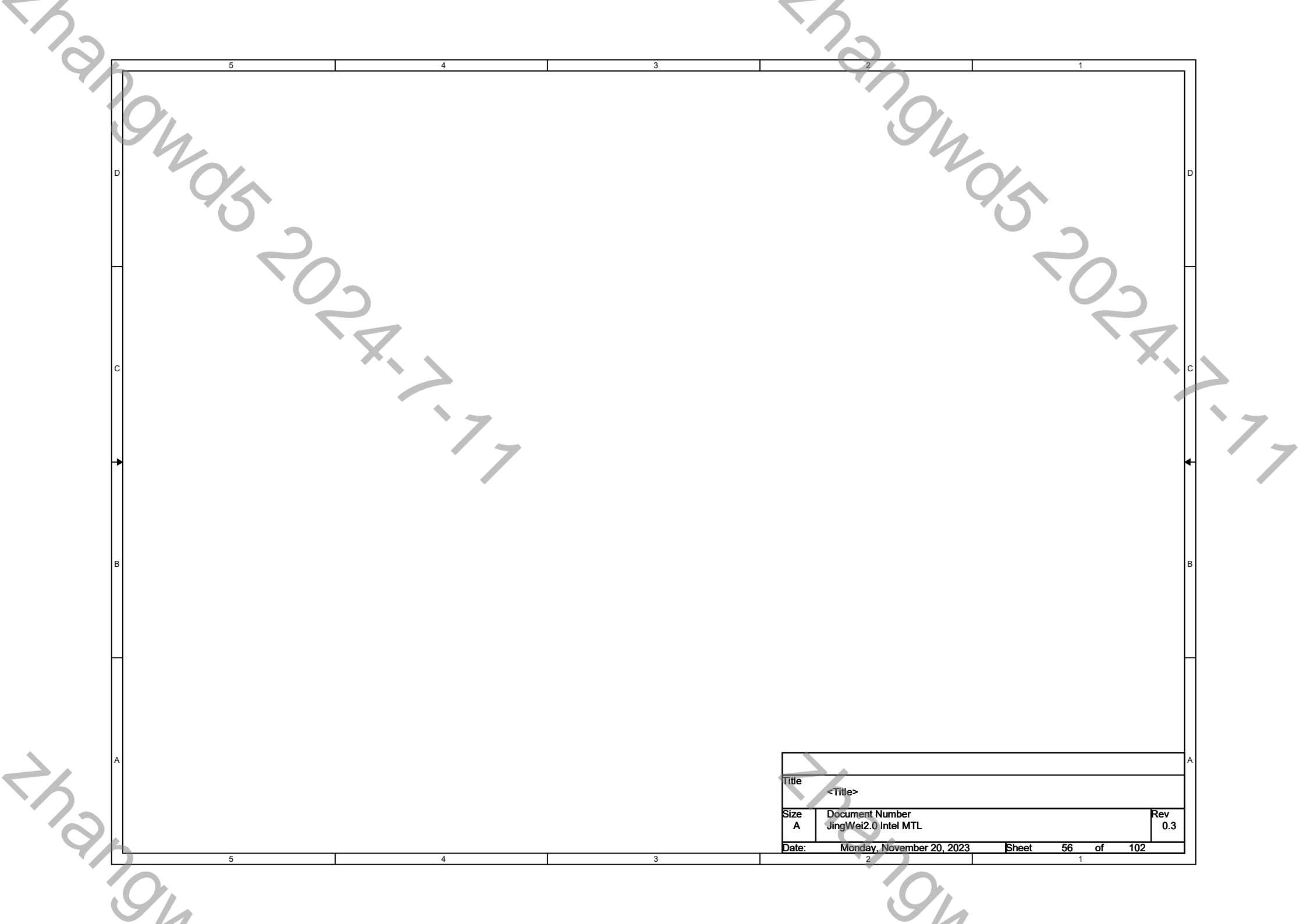
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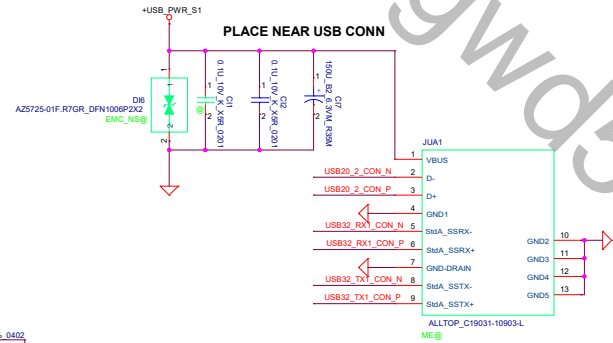
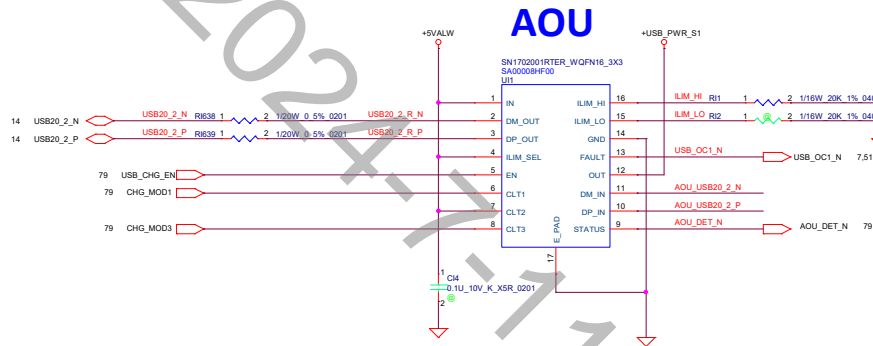
Enable	SELECT			
EN	S1	S0	Y	Function
H	X	X	Hi-Z	Disable
L	L	L	10	S1=0=0
L	L	L	11	S1=0=1
L	H	L	12	S1=0=2
L	H	H	13	S1=0=3



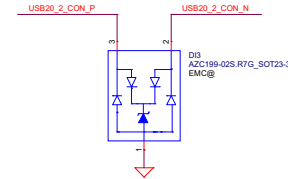
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

Title		
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CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCM OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active




debug circuit delete at 6/21



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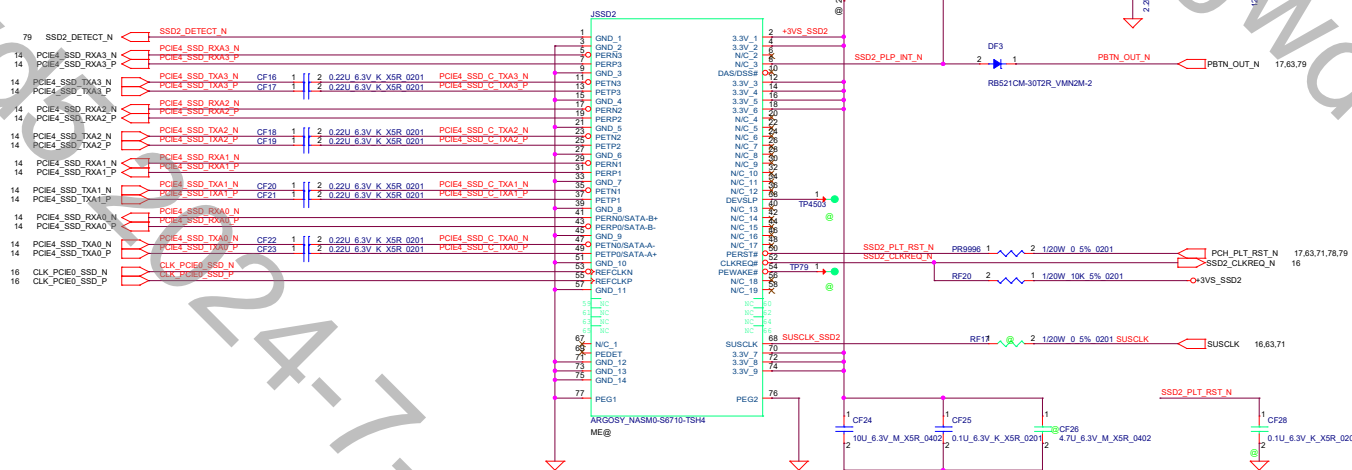
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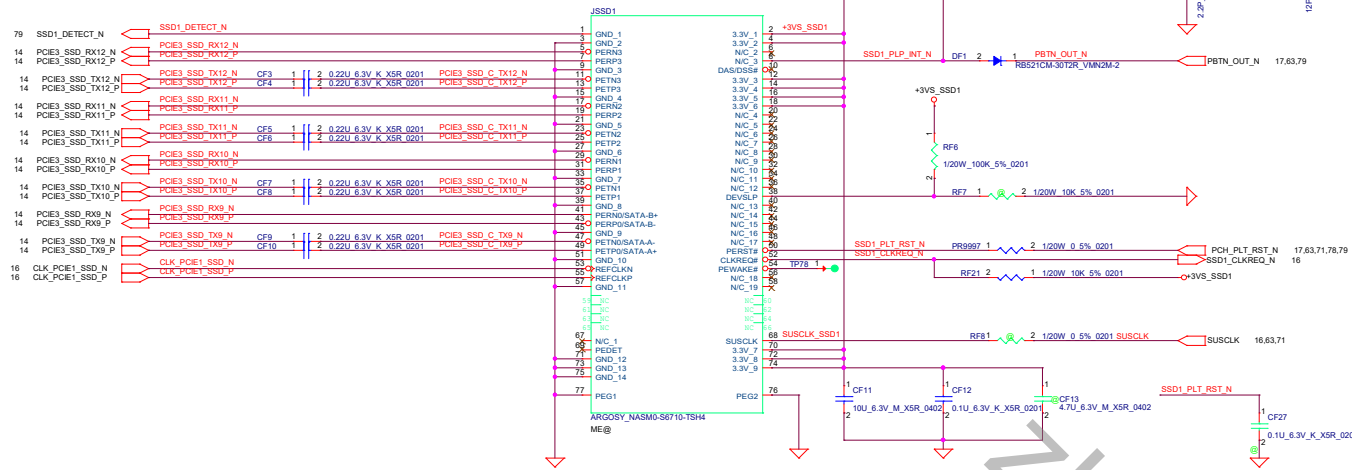
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PCIE GEN4 M.2 SSD(M TYPE) 2280




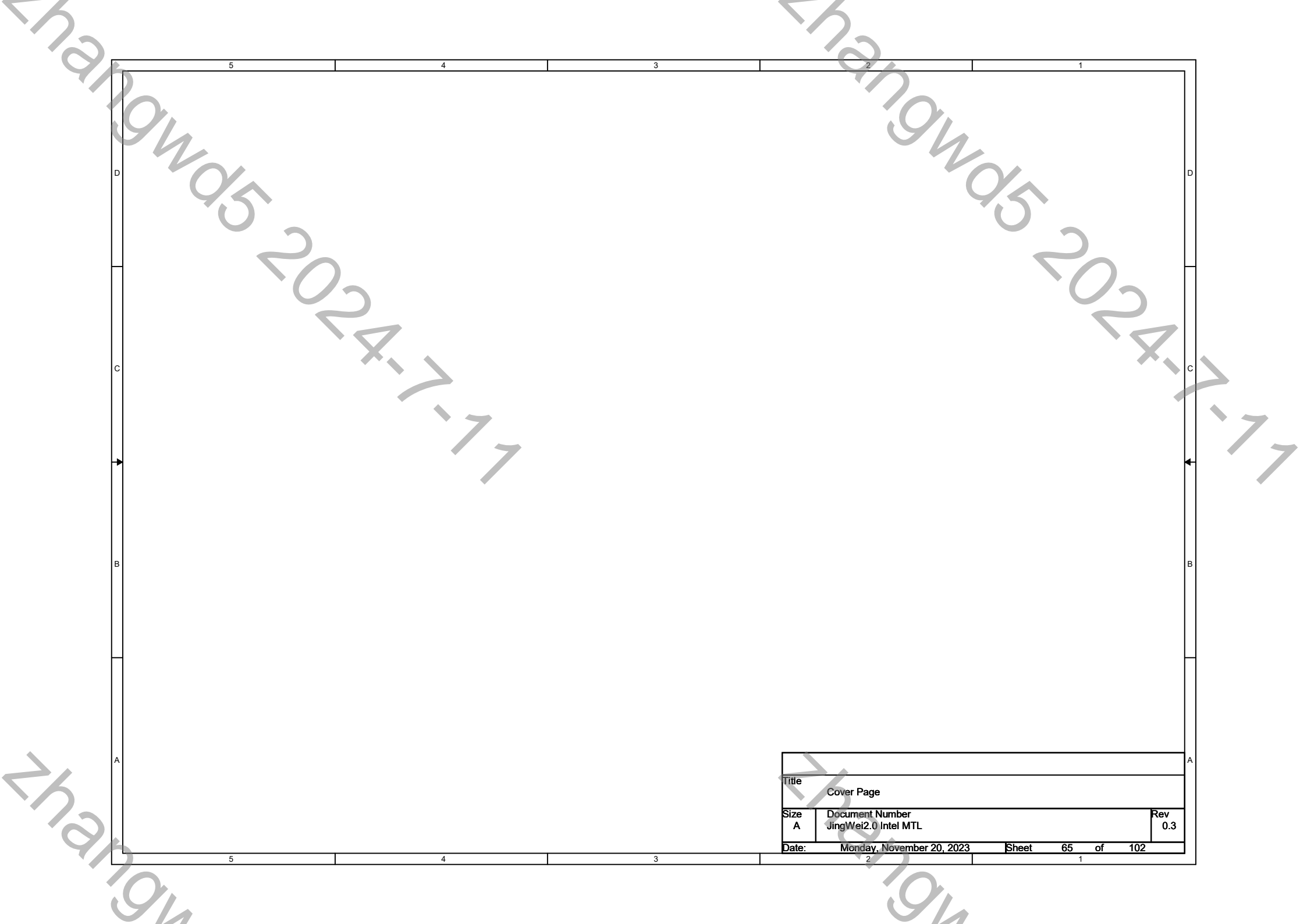
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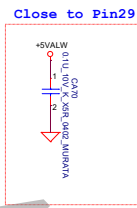
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Apple --> EXT_MIC_A, HGND B
Nokia --> EXT MIC B, HGND A

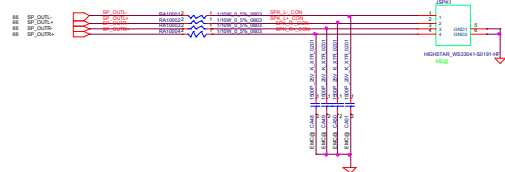
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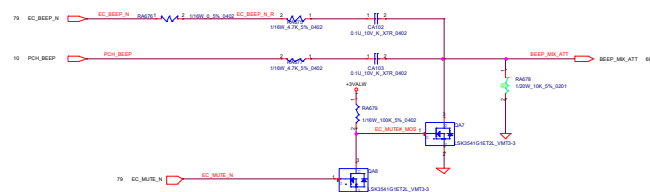
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The schematic diagram illustrates the proposed 6T1R crossbar array architecture. It features a central access transistor (AT) connected to a wordline (WL) and a bitline (BL). The AT's gate is driven by a voltage source \$V_{DD}\$. The AT's source is connected to ground, and its drain is connected to the BL. The BL is also connected to a sense amplifier (SA) circuit, which includes a PMOS transistor (PMOS) and an NMOS transistor (NMOS). The SA's gates are driven by a voltage source \$V_{DD}\$, and their sources are connected to ground. The SA's drains are connected to the BL and a sense output node (SENSE_OUT). The wordline (WL) is connected to a voltage source \$V_{DD}\$ through a resistor (R1). The WL is also connected to a sense output node (SENSE_OUT) through a resistor (R2). The WL is further connected to a sense output node (SENSE_OUT) through a resistor (R3). The WL is also connected to a sense output node (SENSE_OUT) through a resistor (R4).



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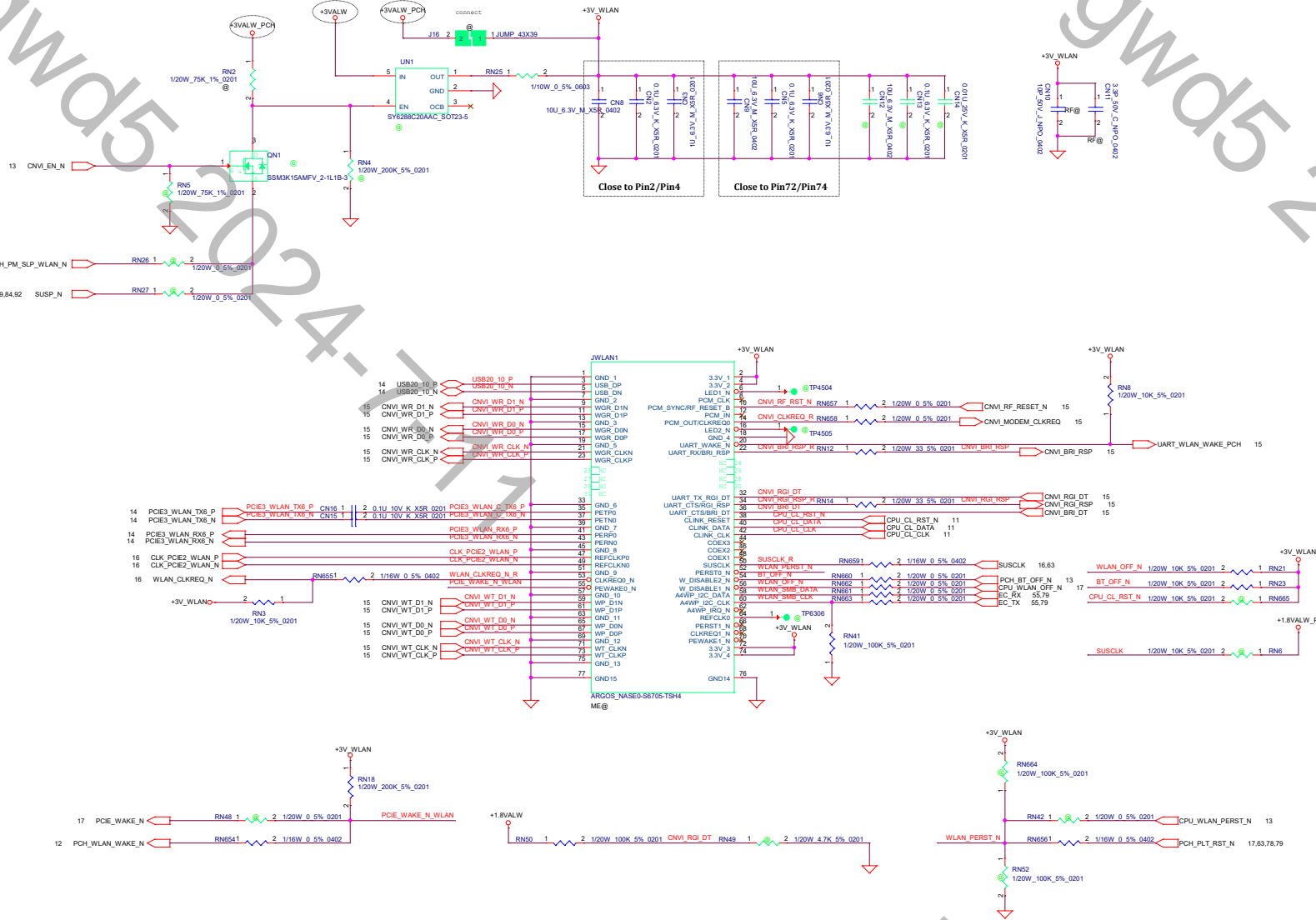
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Mini-Express Card(WLAN/WiMAX)




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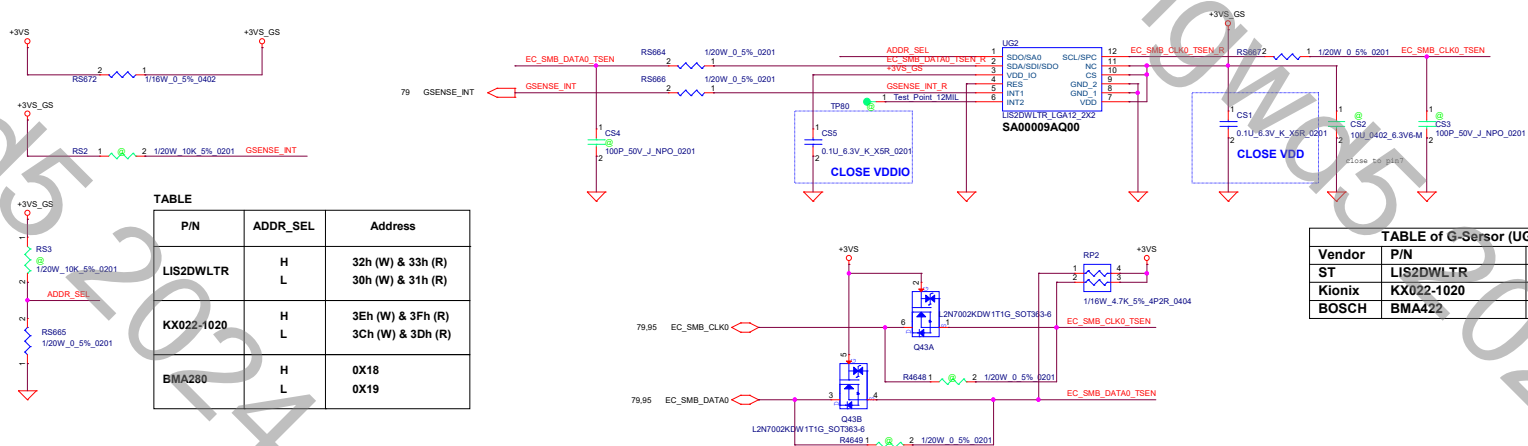
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Size		Document Number		Date		Rev
B		JingWei2.0 Intel MTL		Monday, November 20, 2023		0.3
		Sheet		75 of 102		

APS G-Sensor



Thermal Sensor

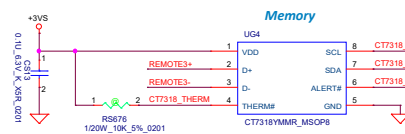
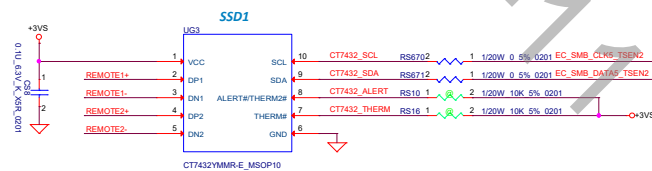
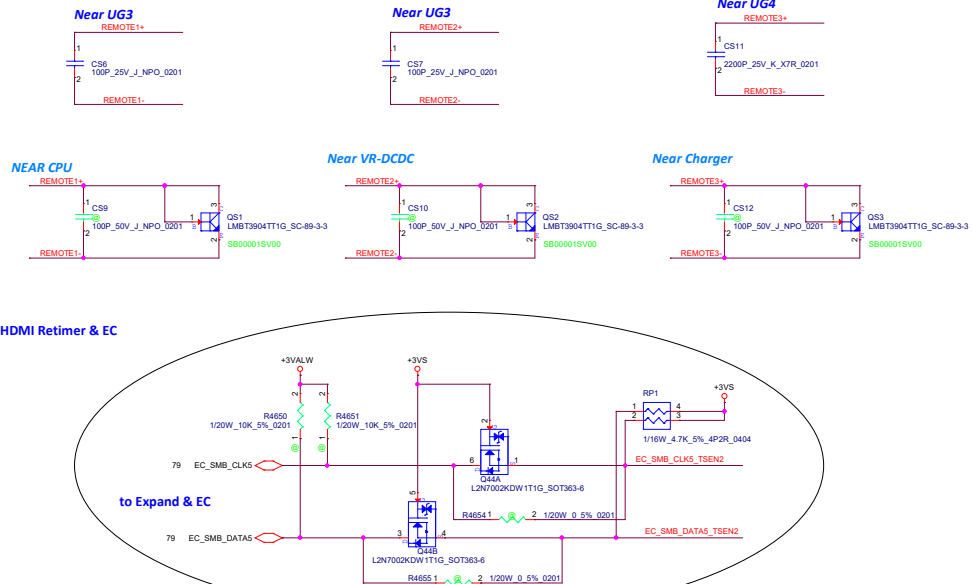
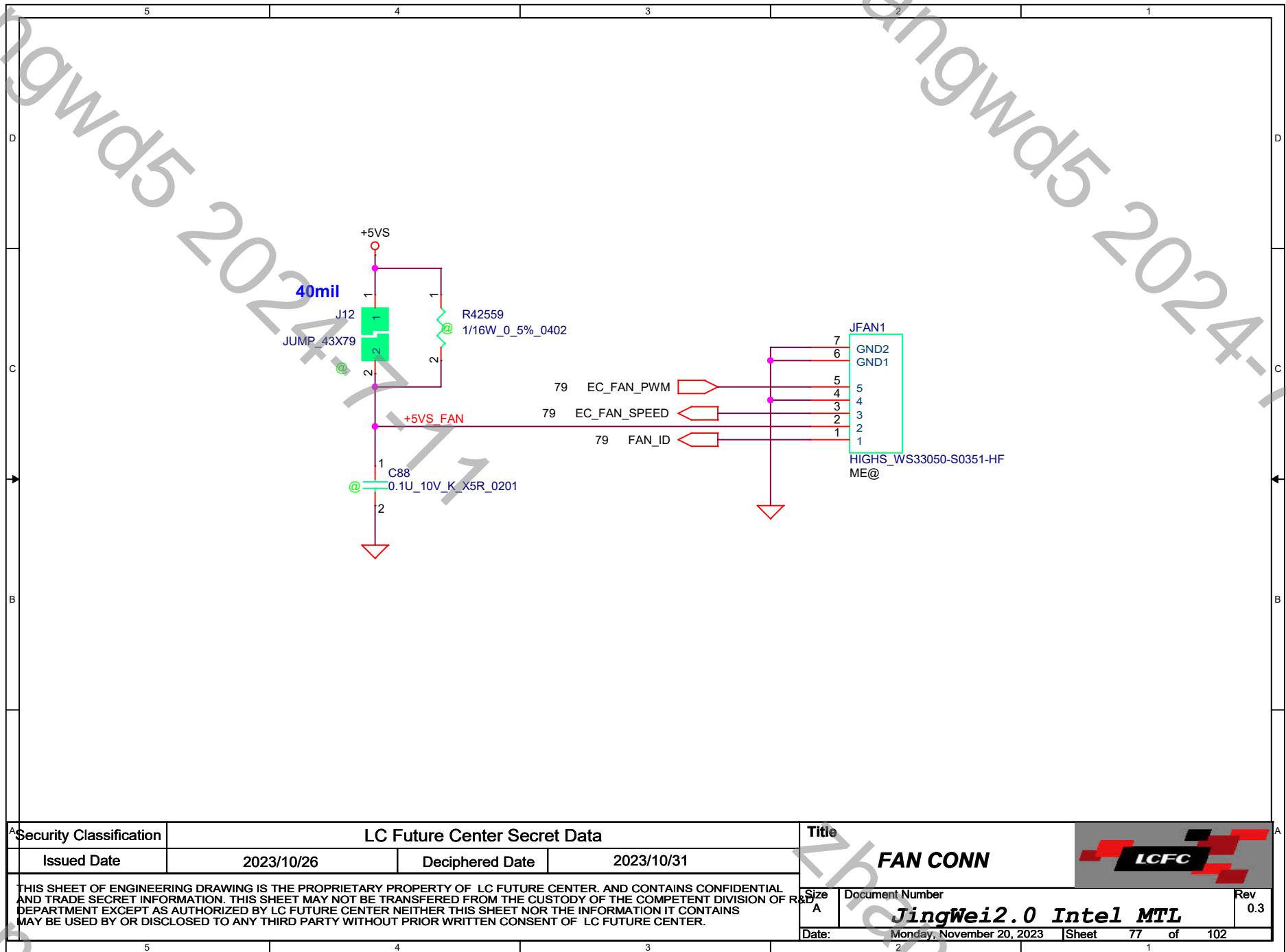


TABLE of Thermal Sensor (UTH1)		
Vendor	LCFC P/N	Description



change at 6/21

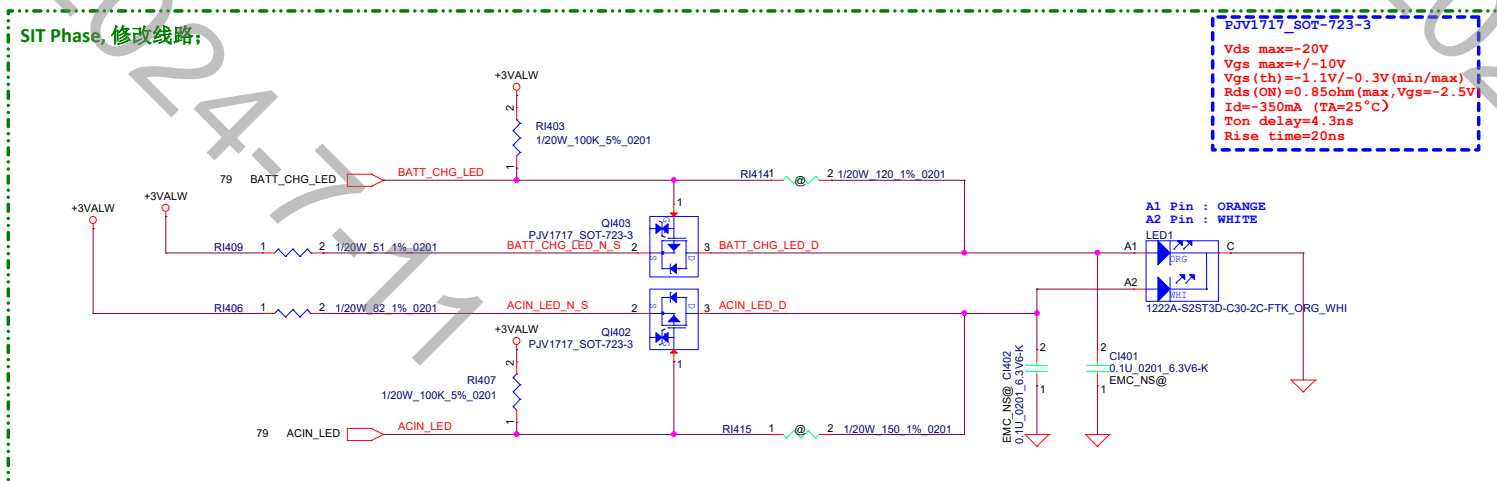
Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		G-SENSOR/Thermal SENSOR	
2023/10/26		2023/10/31		JingWei2.0 Intel MTL	
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		JingWei2.0 Intel MTL		8.3	
		Date		Monday, November 20, 2023	
		Sheet		76 of 102	



Vcc	3.3V
BUS1	10k +/- 5%
SD1 DETECT#	1.98V
SD1 DETECT#	1.772V
SD1 DETECT#	1.675V
SD1 DETECT#	2.533V
SD1 DETECT#	1.755V
SD1 DETECT#	3.3V
SD1 DETECT#	1.524V
SD2 DETECT#	X
SD2 DETECT#	X
SD2 DETECT#	X
SD2 DETECT#	X
SD2 DETECT#	X
SD2 DETECT#	X
SD2 DETECT#	X

Security Classification	LC Future Center Secret Data
Version	2023/10/26
Document Date	2023/10/26
Doc No.	EC-IT227E-256FX
Doc Title	JingWei2.0 Intel MTL
Doc Author	Intel

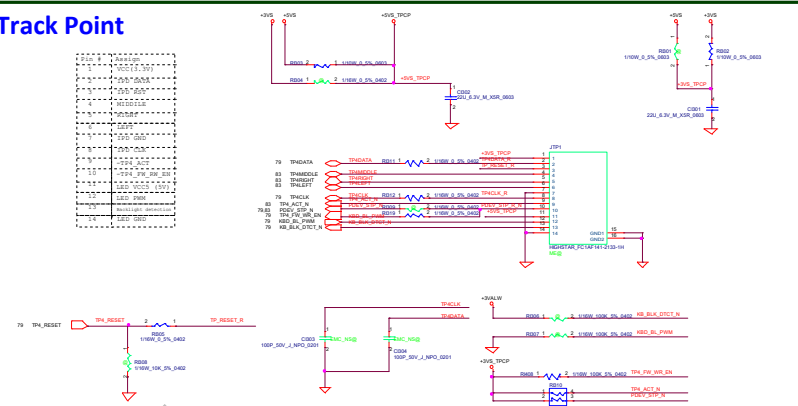
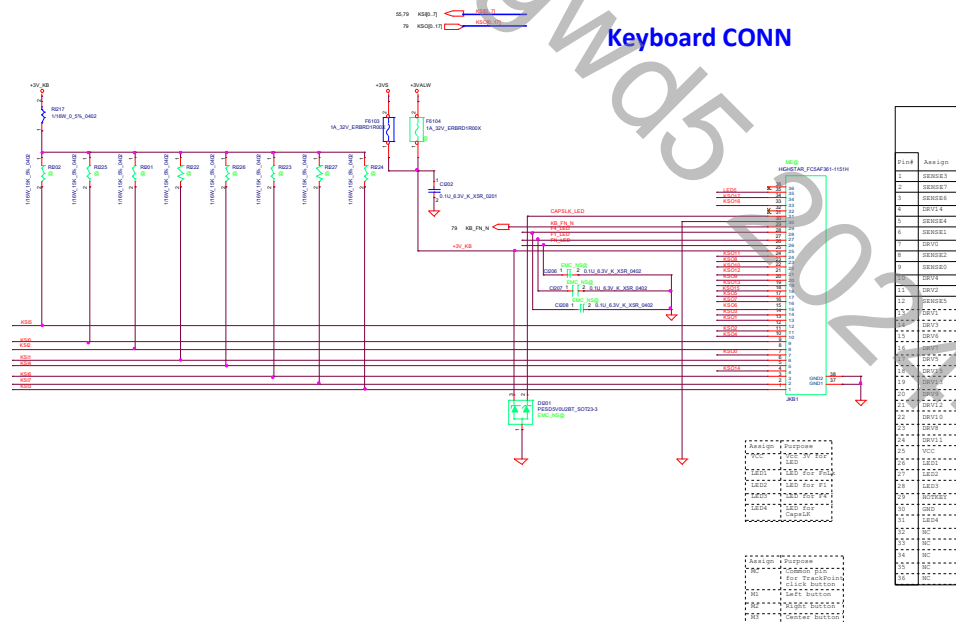
SIT Phase, 修改线路;



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Issued Date	2023/10/26	Deciphered Date	2023/10/31
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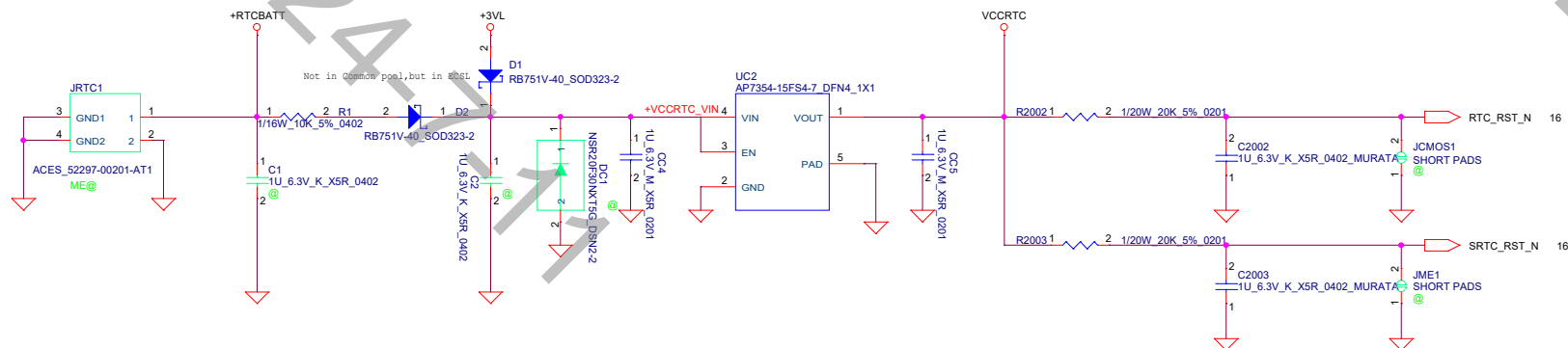
Title		JingWei2.0 Intel MTL	
Power LED		Rev 0.3	
Document Number		Monday, November 20, 2023	
Date:		Sheet 80 of 102	

Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInP	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	



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		2023/10/31		KB/TrackPoint CONN	
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RTC BATTERY



Security Classification	LC Future Center Secret Data			Title	RTC BATTERY	
Issued Date	2023/10/26	Deciphered Date	2023/10/31	Document Number	JingWei2.0 Intel MTL	
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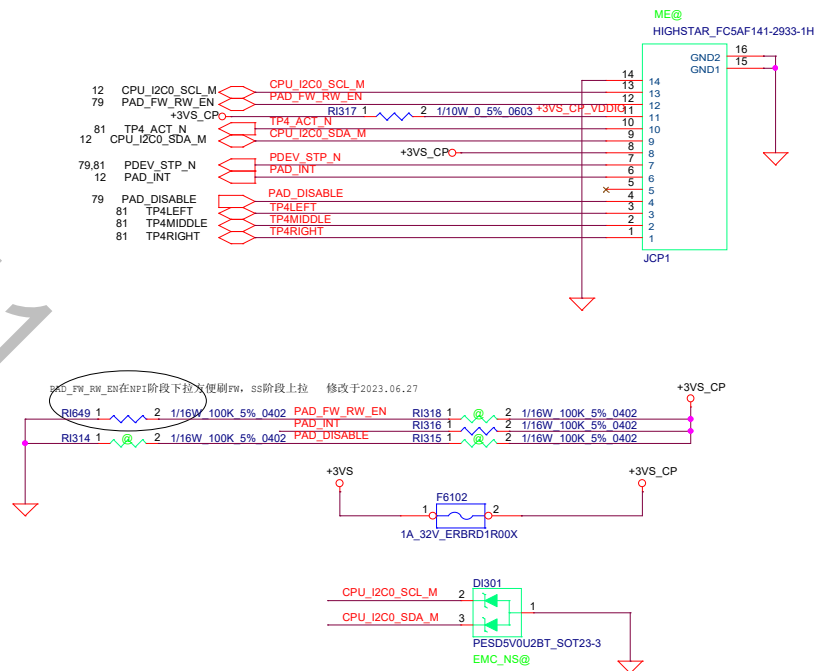
Touch Pad


MB CONN

Pin #	Assign
14	GND
13	I2C_CLK
12	~PAD_FW_RW_EN
11	VDDIO
10	~TP4_ACT
9	I2C_DATA
8	VDD
7	~PDEV_STP
6	~I2C_INT
5	NC
4	PAD_DISABLE
3	TP4LEFT
2	TP4MIDDLE
1	TP4RIGHT

TouchPad CONN


Pin #	Assign
1	GND
2	I2C_CLK
3	-PAD_FW_RW_EN
4	VDDIO
5	-TP4_ACT
6	I2C_DATA
7	VDD
8	-PDEV_STP
9	-I2C_INT
10	NFC_ACTIVE
11	PAD_DISABLE
12	TP4LEFT
13	TP4MIDDLE
14	TP4RIGHT



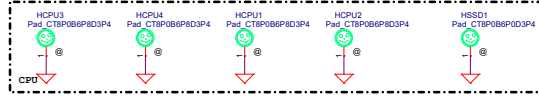
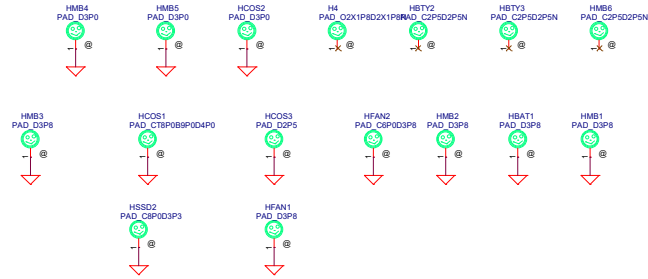
Security Classification				LCFC Highly Confidential Information				Title		
Issued Date		2023/10/26		Deciphered Date		2023/10/31		TouchPad CONN		
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Document Number		JingWei2.0 Intel MTL								Rev 0.3
Date		Monday, November 20, 2023				Sheet		83 of 102		

Vout (V)	R1 (K Ω)	R2 (K Ω)
3.52V	34	10
$V_{OUT} = 0.8 \times (1 + R1/R2)$		

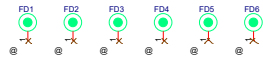
zhangwd5 2024-7-11

Security Classification	LC Future Center Secret Data			Title		
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				C	JingWei2.0 Intel MTL	0.3
				Date:	Monday, November 20, 2023	Sheet 85 of 100

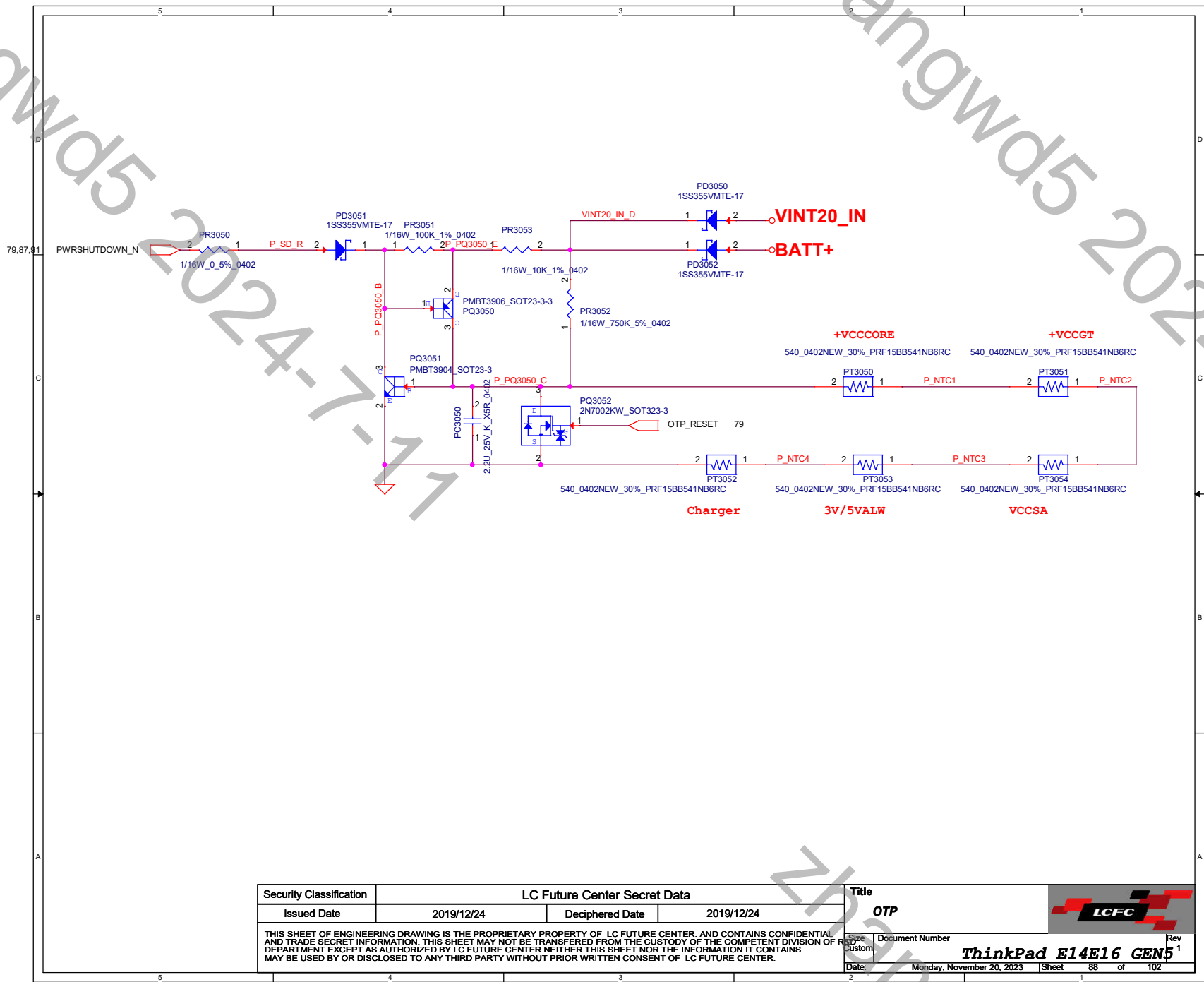
Screw Hole



PCB Federal Mark PAD

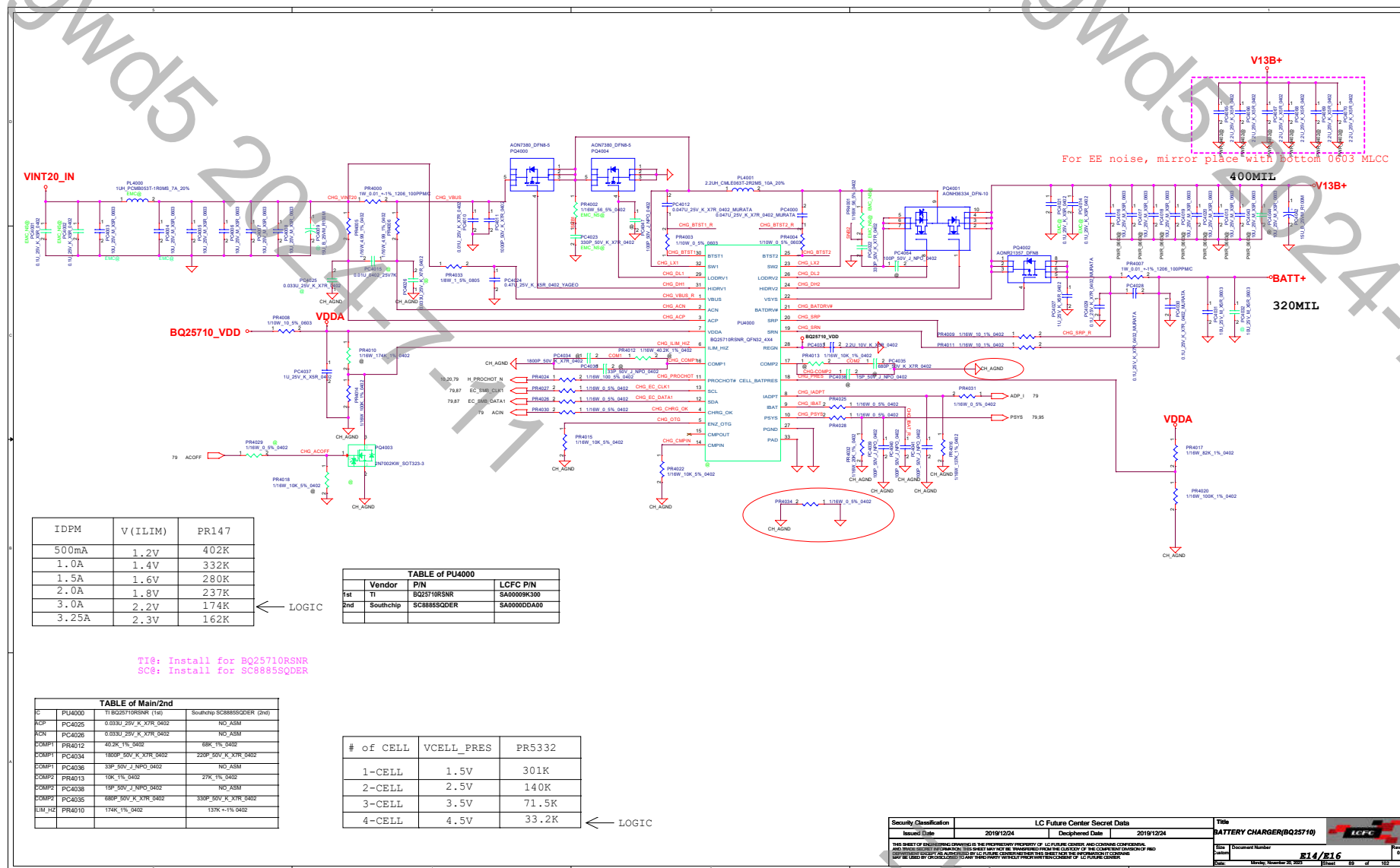



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				Date	Monday, November 20, 2023	Sheet 86 of 102



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Issued Date	2019/12/24	Deciphered Date	2019/12/24
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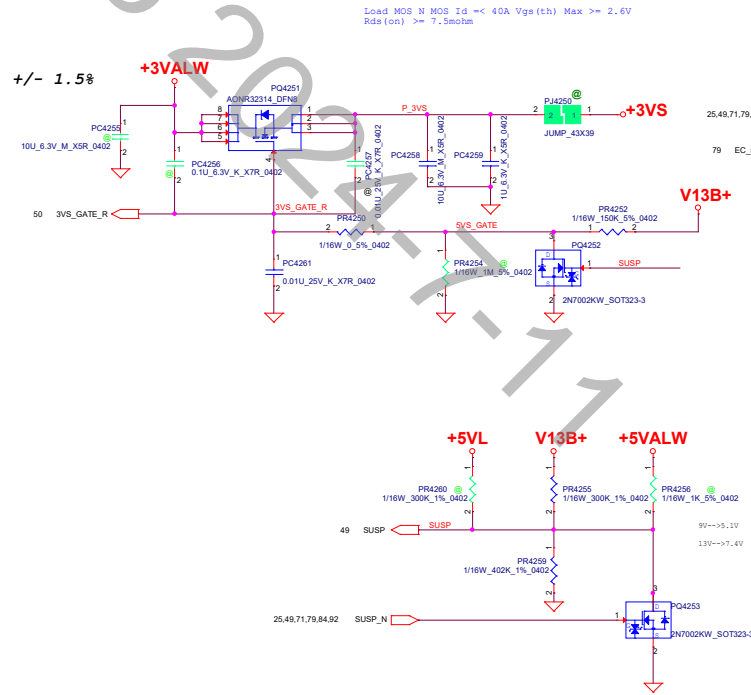
Title			
OTP			
Size	Document Number	Rev	
Custom	ThinkPad E14E16 GEN5	1	
Date:	Monday, November 20, 2023	Sheet	88 of 102



		5	4	3	2	1	
D							D
C							C
B							B
A							A
Security Classification		LC Future Center Secret Data				Title	
Issued Date		2019/12/24	Deciphered Date		2019/12/24	NA	
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		5	4	3	2	1	

+3VS load Switch

+3VALW to +3VS 6.2A request
VSYS15 9V--13V



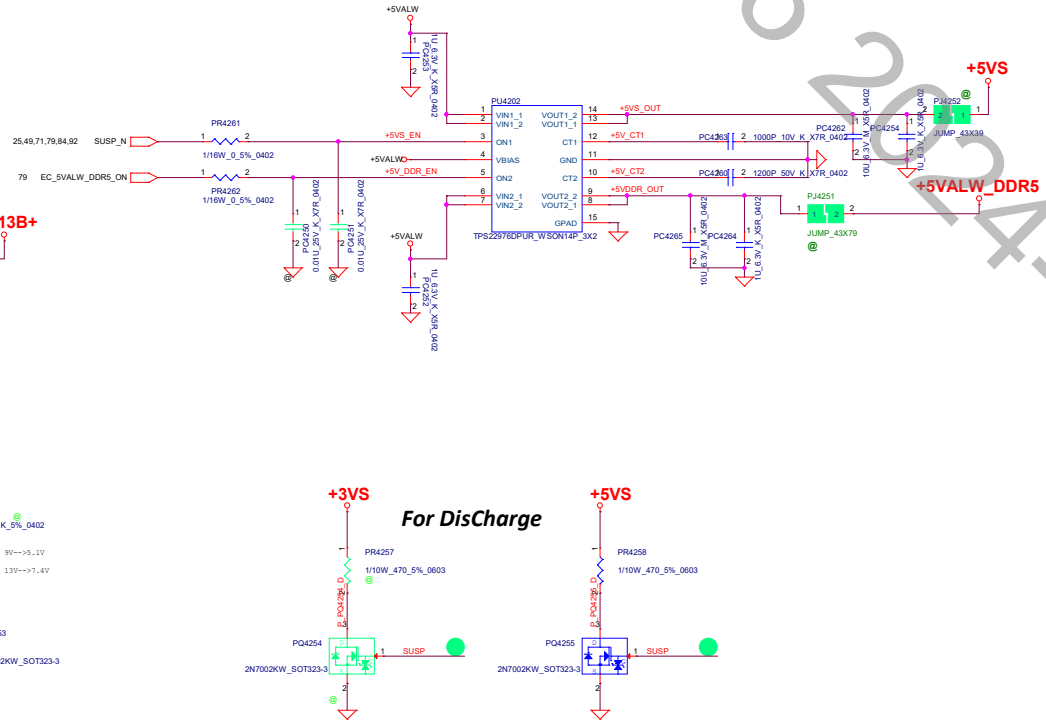
+5VALW_DDR5 load Switch

+5VALW to +5VALW_DDR5 4A request

+5VS load Switch

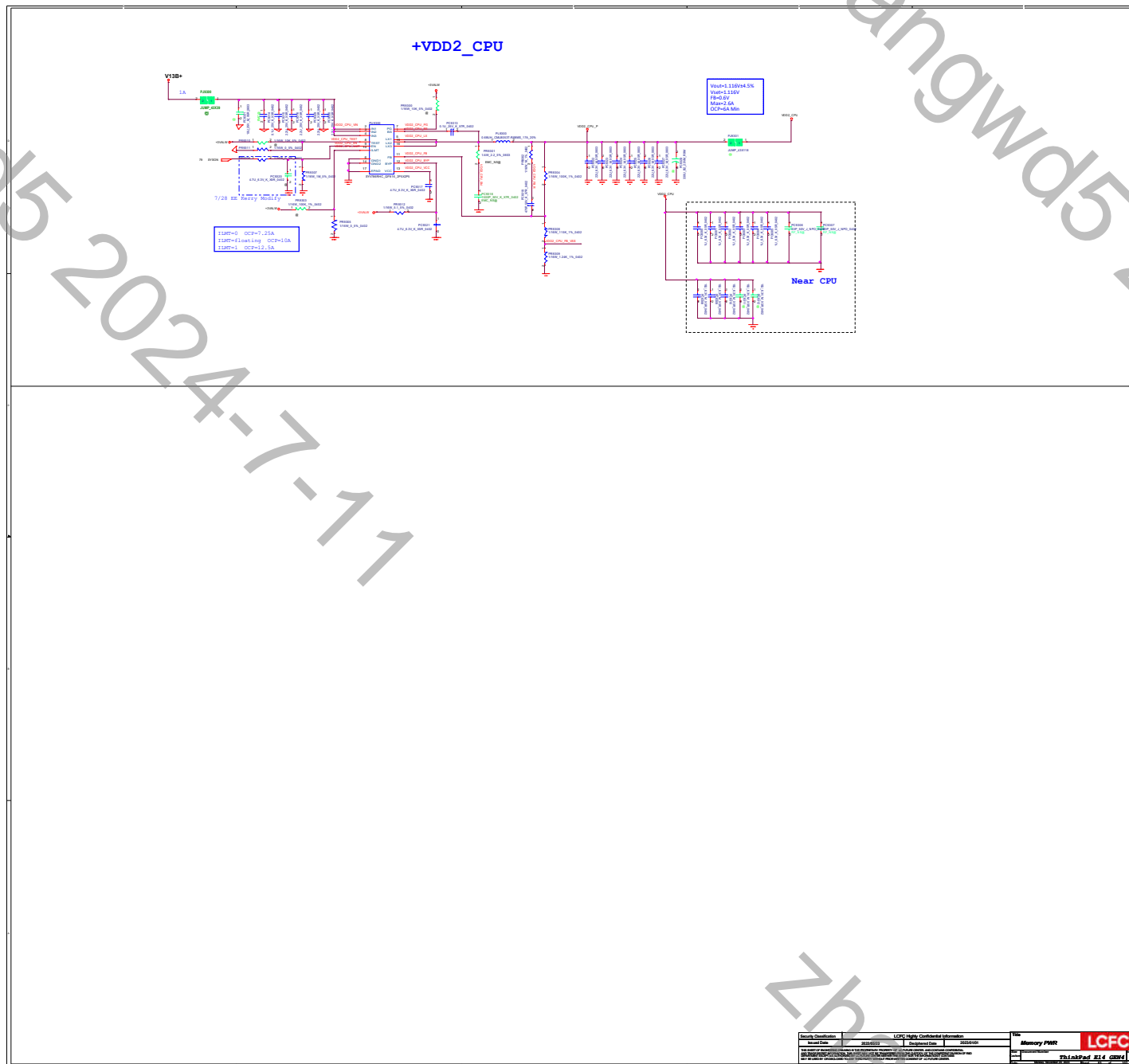
+5VALW to +5VS 2.6A request

Load MOS N MOS Id < 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm



For DisCharge

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			ThinkPad E14 GEN4
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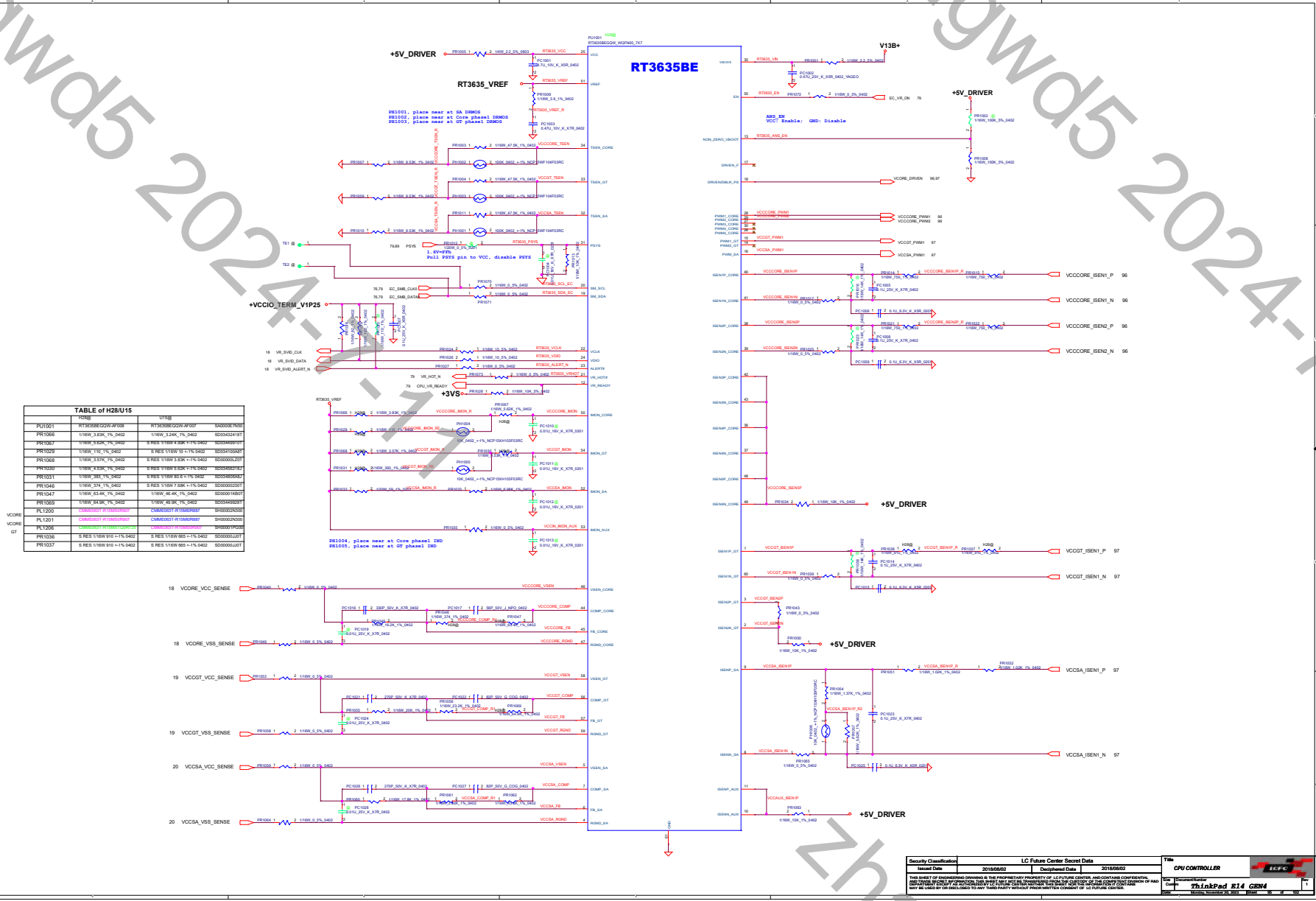


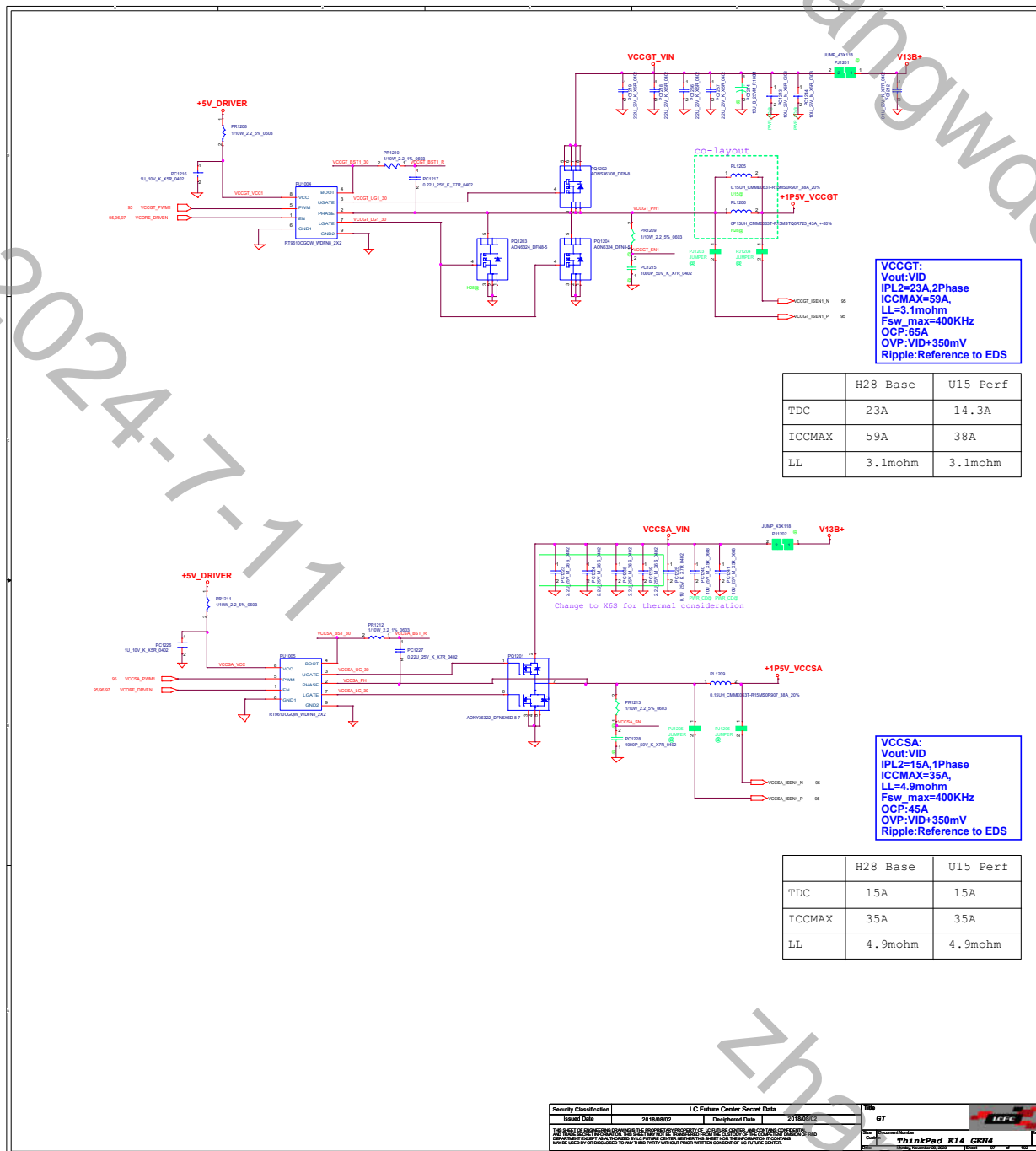
zhangwd5 2024-7-11

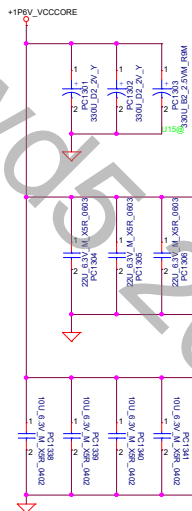
Security Classification	LCFC Highly Confidential Information			Title	LPDDR5 Decoupling		LCFC
Issued Date	2021/01/19	Deciphered Date	2022/01/19	Size	Document Number	Rev	
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TABLE OF H28/U16	
REF ID	REF ID
PR1001	1/10W, 0.83K, 1%, 0.402
PR1006	1/10W, 0.83K, 1%, 0.402
PR1007	1/10W, 0.83K, 1%, 0.402
PR1009	1/10W, 0.83K, 1%, 0.402
PR1010	1/10W, 0.83K, 1%, 0.402
PR1011	1/10W, 0.83K, 1%, 0.402
PR1012	1/10W, 0.83K, 1%, 0.402
PR1013	1/10W, 0.83K, 1%, 0.402
PR1014	1/10W, 0.83K, 1%, 0.402
PR1015	1/10W, 0.83K, 1%, 0.402
PR1016	1/10W, 0.83K, 1%, 0.402
PR1017	1/10W, 0.83K, 1%, 0.402
PR1018	1/10W, 0.83K, 1%, 0.402
PR1019	1/10W, 0.83K, 1%, 0.402
PR1020	1/10W, 0.83K, 1%, 0.402
PR1021	1/10W, 0.83K, 1%, 0.402
PR1022	1/10W, 0.83K, 1%, 0.402
PR1023	1/10W, 0.83K, 1%, 0.402
PR1024	1/10W, 0.83K, 1%, 0.402
PR1025	1/10W, 0.83K, 1%, 0.402
PR1026	1/10W, 0.83K, 1%, 0.402
PR1027	1/10W, 0.83K, 1%, 0.402
PR1028	1/10W, 0.83K, 1%, 0.402
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PR1033	1/10W, 0.83K, 1%, 0.402
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PR1036	1/10W, 0.83K, 1%, 0.402
PR1037	1/10W, 0.83K, 1%, 0.402

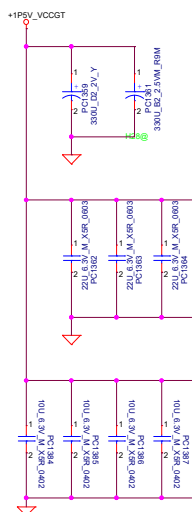
VCCIO
UT







Follow PDG v1.1:
 330uF_7343*3, 47uF_0603*16, 10uF_0402*15
 Actual Stuff:
 330UF B2*1/330UF B2*1/22UF_0603*24, 10UF_0402*15



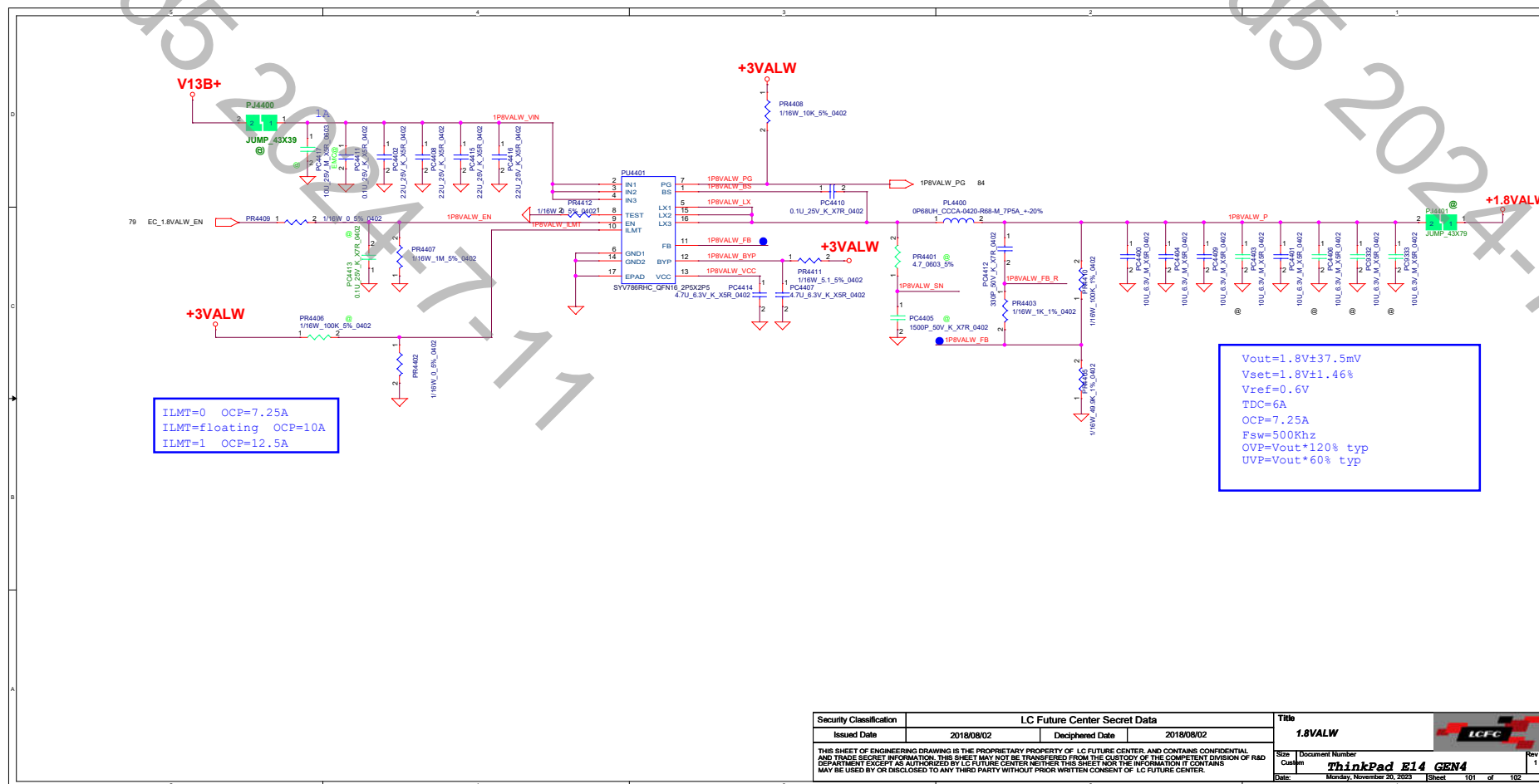
Follow PDG v1.1:
 330uF_7343*(2+1@), 47uF_0603*(4+6@), 22uF_0402*(4+4@), 10uF_0402*6
 Actual Stuff:
 330UF D2*1/330UF B2*1/22UF_0603*20, 10UF_0402*8

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				C
				Document Number
				P098-PWR CPU PWR Decoupling
				Rev
				1.0
				Date
				Monday, November 20, 2023
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+VCCIN_AUX

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Issued Date	2018/08/02	Deciphered Date	2018/08/02	VCCIN_AUX	
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				Custom	ThinkPad E14 GEN4
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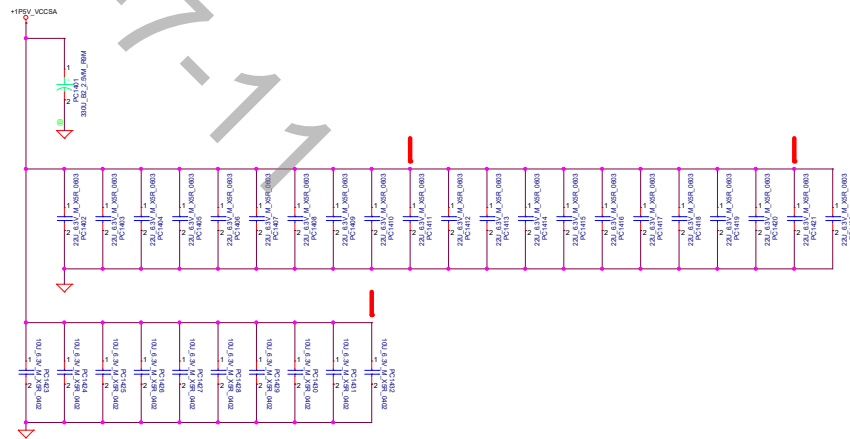


Follow PDG v1.1:

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Actual Stuff:













































330UF B2*0, 22UF_0603*15, 10UF_0402*8



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	PCH Decoupling	
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				ThinkPad E14 GEN4	1
				Issue	1









X76 BOM

Charger TI

 AL1 GROUP PARTS CHARGER TI X76APJ01003	 S.RES 110W 10K ±1% 0402 BQ22110ESNR_QFN32_454 S000000030	 S.RES 110W 40.2K ±1% 0402 PR4012 T4B S003410001	 S.RES 110W 174K ±1% 0402 PR4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001	 S.CER CAP 33P 50V J NPO 0402 PC4012 T4B S003410001
 AL1 GROUP PARTS CHARGER SC X76APJ01004	 S.C. SC8885CODER QFN32P CO P0002 SCB S000000000	 S.RES 110W 27K ±1% 0402 P0002 SCB S003421001	 S.RES 110W 68K ±1% 0402 P0002 SCB S003421001	 S.RES 110W 137K ±1% 0402 P0002 SCB S003421001	 S.CER CAP 330P 50V K X7R 0402 P0002 SCB S003421001	 S.CER CAP 330P 50V K X7R 0402 P0002 SCB S003421001	 S.CER CAP 330P 50V K X7R 0402 P0002 SCB S003421001	 S.CER CAP 330P 50V K X7R 0402 P0002 SCB S003421001	 S.CER CAP 330P 50V K X7R 0402 P0002 SCB S003421001	 S.CER CAP 330P 50V K X7R 0402 P0002 SCB S003421001	 S.CER CAP 330P 50V K X7R 0402 P0002 SCB S003421001
 AL1 GROUP PARTS VCORE MOS AC X76APJ01005	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100	 ACN0334 0FN-5 P0101 AOB S000001100
 AL1 GROUP PARTS VCORE MOS NIKO X76APJ01006	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000	 ACN0334 0FN-5 P0101 NKO S000000000
 AL1 GROUP PARTS VCORE MOS SINOPW X76APJ01007	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000	 S0A0330000C P0101 SNOPOWER S000000000

BOM Structure

U15 CPU install

 PT3038EQWAF007 S000000000	 110W 3.5K ±1% 0402 PR1002 U15B S003404001	 110W 4.5K ±1% 0402 PR1002 U15B S003404001	 110W 10 ±1% 0402 PR1002 U15B S003404001	 110W 3.5K ±1% 0402 PR1002 U15B S003404001	 110W 3.5K ±1% 0402 PR1002 U15B S003404001	 110W 3.5K ±1% 0402 PR1002 U15B S003404001	 110W 3.5K ±1% 0402 PR1002 U15B S003404001	 110W 7.5K ±1% 0402 PR1002 U15B S003404001	 110W 45.4K ±1% 0402 PR1002 U15B S003404001	 110W 55 ±1% 0402 PR1002 U15B S003404001	 110W 55 ±1% 0402 PR1002 U15B S003404001	 110W 55 ±1% 0402 PR1002 U15B S003404001
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